8Gb (x8) – DDR4 Synchronous DRAM
Product Brief

INSIGNIS TECHNOLOGY CORPORATION

1024M x 8 bit DDR4 Synchronous DRAM

Overview

The DDR4 SDRAM is a high-speed dynamic random-access memory internally organized with sixteen- banks (4 bank groups each with 4 banks). The DDR4 SDRAM uses a 8n prefetch architecture to achieve high- speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one- half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Activate Command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate Command are used to select the bank and row to be activated (BG0- BG1 select the bank group; BA0- BA1 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

Features

- JEDEC Standard Compliant
- Fast clock rate: 1333/1600MHz
- Power supplies:
  - V_{DD} & V_{DDQ} = +1.2V ± 0.06V
  - V_{PP} = +2.5V -0.125V / +0.25V
- Operating temperature range:
  - Extended Test (ET): T_C = 0~95°C
  - Industrial Temp (IT): T_C = -40~95°C
- Supports JEDEC clock jitter specification
- Bidirectional differential data strobe, DQS &DQS#
- Differential Clock, CK & CK#
- 16 internal banks: 4 groups of 4 banks each
- Separated IO gating structures by Bank Group
- 8n-bit prefetch architecture
- Precharge & Active power down
- Auto Refresh and Self Refresh
- Low-power auto self refresh (LPASR)
- Self Refresh Abort
- Fine Granularity Refresh
- Write Leveling
- DQ Training via MPR
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command/Address (CA) Parity
- Data bus write cyclic redundancy check (CRC)
- Maximum Power Saving Mode (MPSM)
- Internal V_{REFDQ} Training
- Read Preamble Training
- Control Gear Down Mode
- Per DRAM Addressability (PDA)
- Output Driver Impedance Control
- Dynamic ODT (R_{TT_PARK} & R_{TT_Nom} & R_{TT_WR})
- Input Data Mask (DM) and Data Bus Inversion (DBI)
- ZQ Calibration
- Command/Address latency (CAL)
- Asynchronous Reset
- DLL enable/disable
- Burst Length (BL8/BC4/BC4 or 8 on the fly)
- Burst type: Sequential / Interleave
- CAS Latency (CL)
- CAS Write Latency (CWL)
- Additive Latency (AL): 0, CL-1, CL-2
- Average refresh period
  - 8192 cycles/64ms (7.8us at -40°C ≦ T_C ≦ +85°C)
  - 8192 cycles/32ms (3.9us at +85°C ≦ T_C ≦ +95°C)
- Data Interface: Pseudo Open Drain (POD)
- RoHS compliant
- Hard post package repair (hPPR)
- Soft post package repair (sPPR)
- 78-ball 7.5 x 10.5 x 1.2mm FBGA package
  - Pb and Halogen Free

How to Order

Function	Density	IO Width	Pkg Type	Pkg Size	Speed & Latency	Option	INSIGNIS PART NUMBER:
DDR4	8Gb	x8	FBGA	7.5x10.5 (x1.2)	2666-19-19-19*	Extended Test	NDQ88PFR-7NET
DDR4	8Gb	x8	FBGA	7.5x10.5 (x1.2)	2666-19-19-19*	Industrial Temp	NDQ88PFR-7NIT
DDR4	8Gb	x8	FBGA	7.5x10.5 (x1.2)	3200-22-22-22*	Extended Test	NDQ88PFR-6NET
DDR4	8Gb	x8	FBGA	7.5x10.5 (x1.2)	3200-22-22-22*	Industrial Temp	NDQ88PFR-6NIT

* Backward compatible with slower speed rates.

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