

# 4Gb (x8) - DDR3/DDR3L Synchronous DRAM

## Product Brief



### 512M x 8 bit DDR3/3L Synchronous DRAM

#### Overview

The 4Gb Double-Data-Rate-3L (DDR3L) DRAM is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAM.

The 4Gb chip is organized as 64Mbit x 8 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin for general applications.

The chip is designed to comply with all DDR3L DRAM key features, including full backward compatibility to DDR3. Hereafter the device will be referred to as DDR3L for both part numbers. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks and inputs are latched at the cross point of differential clocks (CK rising and CK# falling). All I/Os are synchronized with differential DQS pair in a source synchronous fashion.

These devices operate with a single +1.35V-0.067V / +0.1V power supply and are available in BGA packages.

#### Features

- JEDEC Standard Compliant
- AEC-Q100 Compliant
- Power supplies:  $V_{DD}$  &  $V_{DDQ} = +1.35V$
- Backward compatible to  $V_{DD}$  &  $V_{DDQ} = +1.5V \pm 0.075V$
- Operating temperature range:
  - Extended Test (ET):  $T_C = 0 \sim 95^{\circ}C$
  - Industrial (IT):  $T_C = -40 \sim 95^{\circ}C$
  - Automotive (AT):  $T_C = -40 \sim 105^{\circ}C$
- Supports JEDEC clock jitter specification
- Fully synchronous operation
- Fast clock rate: 800/933MHz
- Differential Clock, CK & CK#
- Bidirectional differential data strobe
  - DQS & DQS#
- 8 internal banks for concurrent operation
- 8n-bit prefetch architecture
- Pipelined internal architecture
- Precharge & active power down
- Programmable Mode & Extended Mode registers
- Additive Latency (AL): 0, CL-1, CL-2
- Programmable Burst lengths: 4, 8
- Burst type: Sequential / Interleave
- Output Driver Impedance Control
- Average refresh period
  - 8192 cycles/64ms (7.8us at  $-40^{\circ}C \leq T_C \leq +85^{\circ}C$ )
  - 8192 cycles/32ms (3.9us at  $+85^{\circ}C \leq T_C \leq +95^{\circ}C$ )
  - 8192 cycles/16ms (1.95us at  $+95^{\circ}C \leq T_C \leq +105^{\circ}C$ )
- Write Leveling
- ZQ Calibration
- Dynamic ODT (Rtt\_Nom & Rtt\_WR)
- RoHS compliant
- Auto Refresh and Self Refresh
  - Self refresh function not supported with  $T_C > 95^{\circ}C$
- 78-ball 7.5 x 10.5 x 1.0mm FBGA package
  - Pb and Halogen Free

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**How to Order**

Function	Density	IO Width	Pkg Type	Pkg Size	Speed & Latency	Option	INSIGNIS PART NUMBER:
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1600-11-11-11	Extended Test	NDL48PFR-8KET
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1600-11-11-11	Industrial Temp	NDL48PFR-8KIT
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1600-11-11-11	Automotive Temp	NDL48PFR-8KAT
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1866-13-13-13	Extended Test	NDL48PFR-9MET
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1866-13-13-13	Industrial Temp	NDL48PFR-9MIT
DDR3L*	4Gb	x8	FBGA	7.5x10.5 (x1.0)	1866-13-13-13	Automotive Temp	NDL48PFR-9MAT

\* All 4Gb DDR3 parts (part number NDT48P) are covered by DDR3L (part number NDL48P).

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