Qualification and Reliability Report - eMMC 153Balls Industrial Grade

INSIGNIS TECHNOLOGY CORPORATION

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Product Information

Product Name	eMMC
Ordering Information	NSEC53K004-IT NSEC53K008-IT NSEC53K016-IT NSEC53K002-ITJ NSEC53K004-ITJ NSEC53K008-ITJ
Grade Temperature	Industrial Grade: -40 ~ 85℃
Package	153Balls (11.5x13.0x1.0mm)
Flash Type	15nm MLC (available in p-SLC mode)

Note: NAND Flash Reliability Tests according to Toshiba reliability test report. (Report No.: RTM7150010)

Result Overview

Package Qualification			
Test Item	**Test Reference**	**Sample Size**	**Test Result**
Pre-condition Test (PC)	JEDEC/JESD22-A113	122 units (Before uHAST, TCT)	Pass
High Acceleration Stress Test (HAST/unbias)	JEDEC/JESD22-A118	45 units	Pass
Temperature Cycling Test (TCT)	JEDEC/JESD22-A104	77 units	Pass
High Temperature Storage Life Test (HTSL)	JEDEC/JESD22-A103	45 units	Pass
Solderability (SD)	JESD22-B102	5 units	Pass
Physical Dimension (PD)	JEDEC/JESD22-B100	5 units	Pass
Wire Bond Shear (WBS)	JEDEC/JESD22-B116	5 units, 30 bonds/unit	Pass
Wire Bond Pull (WBP)	MIL-STD-883G, Method 2011.7	5 units, 30 bonds/unit	Pass
Solder Ball Shear (SBS)	JEDEC/JESD22-B117	5 units, 30 balls/unit	Pass
Device Qualification			
Test Item	**Test Reference**	**Sample Size**	**Test Result**
High Temperature Operation Life (HTOL)	JEDEC/ JESD22-A108	3Lots, 77 units/Lot	Pass
ESD Test (Human-Body Model, HBM)	MIL-STD-883G, Method 3015.7	3	Pass
ESD Test (Charged Device Model, CDM)	JEDEC/JESD22-C101	3	Pass
Latch-Up Test (LU)	JESD78	6	Pass

NAND Flash Reliability Tests			
Test Item	**Test Reference**	**Sample Size**	**Test Result**
Write/Erase Endurance Test	JEDEC/JESD22-A117	480	Pass
Data Retention Test	JEDEC/JESD22-A117	231	Pass
Read Disturb	JEDEC/JESD22-A117	80	Pass

Accelerated Environment Stress Test

Pre-condition Test (PC)

Purpose:

This Test Method establishes an industry standard preconditioning flow for non-thematic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

Test Conditions:

- Step1: External Visual & Function Test and SAT Inspection
- Step2: Temperature Cycle Test (-65℃/150℃, 5 cycles)
- Step3: High temperature Storage Baking (125℃, 24 hours)
- Step4: Moisture soak (60℃/60% RH, 40 hours)
- Step5: IR Reflow * 3 times (260℃)
- Step6: External Visual & Function Test and SAT Inspection
- Sample size: 122ea
- Test Reference: JESD22-A113

Test Result:

Product	Result	Remark	Test Part No.
eMMC 153balls	0 Fail/122	N/A	NSEC53K004-IT NSEC53K008-IT NSEC53K064-IT

Criteria: Acc/Rej = 0/1

High Acceleration Stress Test (HAST/unbias)

Purpose:

The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

Test Conditions:

- Pre-condition
- 110°C, 85%RH, 264 hours
- Each device test and all pass by VI and FT
- Sample size: 45ea
- Test Reference: JEDS22-A118

Test Result:

Product	Result	Remark	Test Part No.
eMMC 153balls	0 Fail/45	N/A	NSEC53K004-IT NSEC53K008-IT NSEC53K064-IT

Criteria: Acc/Rej = 0/1

Temperature Cycling Test (TCT)

Purpose:

This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

Test Conditions:

- Pre-condition
- -65°C~150°C, Transition time: 5 minutes, Dwell time = 10 minutes
- Test Duration: 200/ 500 cycles
- Sample size: 77ea
- Test Reference: JEDS22-A104

Test Result:

Product	Result	Remark	Test Part No.
eMMC 153balls	0 Fail/77	N/A	NSEC53K004-IT NSEC53K008-IT NSEC53K064-IT

Criteria: Acc/Rej = 0/1

High Temperature Storage Life Test (HTSL)

Purpose:

The high temperature storage test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time to failure distributions of solid state electronic devices, including non-volatile memory devices (data retention failure mechanisms). Thermally activated failure mechanisms are modeled using the Arrhenius Equation for acceleration. During the test, accelerated stress temperatures are used without electrical conditions applied. This test may be destructive, depending on time, temperature and packaging (if any).

Test Conditions:

- High ambient temperature = 150°C
- Test Duration: 168/ 1000 hours
- Sample size: 45ea
- Test Reference: JESD22-A103

Test Result:

Product	Result	Remark	Test Part No.
eMMC 153balls	0 Fail/45	N/A	NSEC53K004-IT NSEC53K008-IT NSEC53K064-IT

Criteria: Acc/Rej = 0/1

Solderability Test (SD)

Purpose:

The purpose of this test method is to evaluate the solderability of terminations that are normally joined by a soldering operation.

Test Conditions:

- 8 hours steam aging (water vapor 93°C +3°C /-5°C)
- Temperature = 245±5℃
- Dwell time = 5±0.5 sec
- Sample size: 5ea
- Test Reference: JESD22-B102

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	>95% lead coverage of critical areas	Pass	N/A	NSEC53K064-IT

Criteria: Acc/Rej = 0/1

Physical Dimensions (PD)

Purpose:

The test is to measure samples' coplanarity.

Test Conditions:

- Sample size: 5ea
- Test reference: JESD22-B100

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	Cpk>1.33	Pass	N/A	NSEC53K064-IT

Wire Bond Shear (WBS)

Purpose:

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a package bonding surface, or an aluminum wedge/stitch bond and a package bonding surface, on either pre-encapsulation or post-encapsulation devices. This strength measurement is extremely important in determining two features:

1. The integrity of the metallurgical bond which has been formed.
2. The reliability of gold and aluminum wire bonds to die or package bonding surfaces.

Test Conditions:

- 30 bonds from minimum 5 units
- Sample size: 5ea, 30 bonds/ea, Total: 150 bonds
- Test speed: 100um/sec
- Shear height: 3um
- Test minimum bond stress (grams force): bigger than 12.6 grams for wire bond is 0.8mil.
- Test Reference: JESD22-B116

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	Cpk>1.33	Pass	N/A	NSEC53K064-IT

Wire Bond Pull (WBP)

Purpose:

The test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

Test Conditions:

- 30 bonds from minimum 5 units
- Sample size: 5ea, 30 bonds/ea, Total: 150 bonds
- Test speed: 600um/sec
- Test minimum bond stress (grams force): bigger than 1.7 grams for wire bond is 0.8mil.
- Test Reference: MIL-STD-883G, Method 2011

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	Cpk>1.33	Pass	N/A	NSEC53K064-IT

Solder Ball Shear (SBS)

Purpose:

The purpose of this test method is to define the procedure for measuring the shear strength of the interface between the barrier metal and solder ball. This method also establishes the minimum shear strength requirements for this interface.

Test Conditions:

- Sample size: 5ea, 30 balls/ea, Total: 150balls
- Test speed: 280um/sec
- Shear height: 50um
- Ball height: 0.15mm
- Test minimum ball stress (grams force): greater than 197 grams for barrier metal diameter is 0.275mm
- Test Reference: JESD22-B117

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	Cpk>1.33	Pass	N/A	NSEC53K064-IT

Device Qualification

High Temperature Operating Life (HTOL)

Purpose:

The HTOL test is to evaluate the endurance of devices when they are submitted to electrical stress and thermal stress over an extended time period.

Test Conditions:

- High ambient temperature = 125℃
- Test Duration: 1000 hours
- Vstress = 3.63V
- Sample size: 3 Lots, 231ea (77ea/Lot)
- Test Reference: JESD22-A108

Test Result:

Product	Result	Remark	Test Part No.
eMMC 153balls	0 Fail/231	N/A	NSEC53K004-IT NSEC53K008-IT NSEC53K064-IT

Criteria: Acc/Rej = 0/1

ESD Test (Human Body Model, HBM)

Purpose:

This method establishes a standard procedure for testing microcircuits using an electrostatic discharge (ESD) model known commonly in the industry as the Machine Model (MM). The objective is to provide reliable, repeatable MM ESD test results. There is limited data supporting the ability of this model to simulate discharges of machinery or to establish manufacturing handling practices. However, the model is useful for producing human-body model (HBM)-like ESD effects at lower voltages and for failure mode determination. The method produces results with are closely related to HBM and produces similar failure modes.

Test Conditions:

- Resistor: 1.5kΩ, Capacitor: 100 pF
- 500V~ 2000V(±), Step: 250V(±)
- Sample size: 3ea
- Test Reference: MIL-STD-883G, Method 3015.7

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	0 Fails, Class 2: 2000 volts to 3999 volts	Pass	N/A	NSEC53K064-IT

ESD Test (Charged Device Model, CDM)

Purpose:

The purpose is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic devices. This model is for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD). The model is an alternative to the human-body model (HBM).

Test Conditions:

- >=500V
- Sample size: 3ea
- Test Reference: JESD22-C101

Test Result:

Product	Test Criteria	Result	Remark	Test Part No.
eMMC 153balls	0 Fails, Class 3: 500 volts to 1000 volts	Pass	N/A	NSEC53K064-IT

Latch-Up Test (LU)

Purpose:

The latch-up test is to evaluate the immunity of semiconductor devices (mainly CMOS devices) to "latch-up," that is a temporary short-circuiting between the power source and the ground caused by electrical noise coming from I/O and power supply pins of a device through two parasitic bipolar structures before a power supply is removed.

Test Conditions:

- Tigger Current: 100mA~ 200mA(±); Step: 50V(±)
- Over Voltage Test: VDD 2V(±) with Limit: 500mA; VCCQ3V(+) with Limit: 500mA; VCC 5.5V(+) with Limit: 500mA
- Test Temperature: room temp.
- Sample size: 6ea
- Test Reference: JESD78

Test Result:

Test Mode	Test Criteria	Result	Test Part No.
Current Inject Mode	0 Fail, Class I: >=+- 100mA	Pass	NSEC53K064-IT
Over Voltage Mode	0 Fail, Class I>=1.5*Vccmax	Pass	NSEC53K064-IT

Criteria: Acc/Rej = 0/1

NAND Flash Reliability Tests

Write/Erase Endurance Test

Purpose:

The test results described below were obtained using NAND Flash test conditions and are provided for reference purposes and to understand the endurance capacity.

Test Unit:

- 15nm MLC 32GB/64GB/128GB NAND Flash

Test Conditions:

- Ambient temperature = 25°C and 85°C with 3,000 cycles
- Test Reference: JESD22-A117

Test Result:

Test Condition	Sample Size	Number of Cumulative Failed Blocks	Failure Rate of Cumulative Failed Blocks	Result
Tc = 25°C, 3k cycles	240	0	0.000%	Pass
Tc = 85°C, 3k cycles	240	0	0.000%	Pass

Failure Criteria: A block is defined as a failed block if the block fails a status read after either an auto program or auto block erase operation.

Data Retention Test

Purpose:

The test results described below were obtained using NAND Flash test conditions and are provided for reference purposes and to understand the data retention capacity.

Test Unit:

- 15nm MLC NAND Flash

Test Conditions:

- Ambient temperature = 25°C and 85°C with 3,000 cycles
- Test Reference: JESD22-A117

Test Result:

Pre-condition	Test Condition	Sample Size	Number of Failures	Result
Write/Erase Tc = 25°C, 300 cycles	Tc = 25°C, 500hour	114	0	Pass
Write/Erase Tc = 25°C, 3K cycles	Tc = 25°C, 500hour		0	Pass
Write/Erase Tc = 85°C, 300 cycles	Tc = 125°C, 100hour	117	0	Pass
Write/Erase Tc = 55/85°C, 3K cycles	Tc = 125°C, 10hour		0	Pass

Failure Criteria: A chip is defined as a failure if the physical random data that is randomly programmed per cycle is uncorrectable with 40-bit ECC/1024 Bytes and the applicable read retry sequence(s).

Read Disturb

Purpose:

The test results described below were obtained using NAND Flash test conditions and are provided for reference purposes and to understand the data retention capacity.

Test Unit:

- 15nm MLC NAND Flash

Test Conditions:

- Ambient temperature = 25°C and 85°C with 3,000 cycles
- Test Reference: JESD22-A117

Test Result:

Pre-condition	Test Condition	Sample Size	Number of Failures	Result
Write/Erase Initial	Tc = 25°C, Vcc = 3.3V Read 100K/page	40	0	Pass
Write/Erase Tc = 25°C, 3K cycles	Tc = 25°C, Vcc = 3.3V Read 10K/page	40	0	Pass

Failure Criteria: A chip is defined as a failure if the physical random data that is randomly programmed per cycle is uncorrectable with 40-bit ECC per 1024 Bytes and the applicable read retry sequence(s).

Conclusion

All of the samples passed the functional, electrical characteristic, and cosmetic checks before, during and after each reliability test.