

# Insignis DDR4 Speed Grades

# DDR4 speed grades within the speed grades

The DDR4 specifications offers users a wide range of speed grade options. Even after the clock frequency has been selected, there are multiple speed grades under that tCK. DDR4-2400 is an example where there are 4 speed grades defined within the same clock frequency.

| Standard name | Memory clock (MHz) | I/O bus clock (MHz) | Data rate (MT/s) | Module name | Peak transfer rate (MB/s) | Timings CL-tRCD-tRP | CAS latency (ns) |
|---------------|--------------------|---------------------|------------------|-------------|---------------------------|---------------------|------------------|
| DDR4-2400P    | 300                | 1200                | 2400             | PC4-19200   | 19200                     | 15-15-15-15         | 12.5             |
| DDR4-2400R    |                    |                     |                  |             |                           | 16-16-16-16         | 13.32            |
| DDR4-2400T    |                    |                     |                  |             |                           | 17-17-17-17         | 14.16            |
| DDR4-2400U    |                    |                     |                  |             |                           | 18-18-18-18         | 15               |

From the DRAM perspective, how fast the design and process is able to complete the timing critical operations sets the speed of the part. The typical architecture specifications that limit the speed are tAA, tRP and tRCD. These are all array functions that are tuned to be optimized for what the process drive capabilities versus capacitance loads will allow. From the chart above it shows that early generation and slower designs on older process nodes will operate at the slower speed grade like DDR4-2400T where the new designs and process nodes will operate at the faster speed grade DDR4-2400R.

But what is the real advantage in the system for the faster speed grades? The memory clock is running at the same frequency, which means that data is being burst out of the DRAM at the same speed, so what is the benefit? The benefit for the example above is that there is one fewer clock cycle for tAA, tRP and tRCD, which cuts those specs down by .83ns each. However, in a typical usage model over many seconds or minutes, the number of tAA, tRP and tRCD cycles are small in comparison to the other functions within the system and on the DRAM. Every usage model is different, but in our experience across thousands of different usage models, the expected system performance gain from one clock cycle faster tAA, tRP and tRCD on a typical model is up to a 0.1% performance difference. Of course, if your system can run a speed test on the memory installed, this would simplify vendor choice.