16M x 32 bit LPDDR Synchronous DRAM

Overview

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory (DRAM) organized as 16M x 32 and containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bits banks is organized as 8,192 rows by 512 columns by 32 bits. These devices feature advanced circuit design to provide low active current and extremely low standby current. The device is compatible with the JEDEC standard Low Power DDR SDRAM specifications.

The 512Mb Low Power DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer four data words per clock cycle at the I/O balls. A single read or write access for the 512Mb DDR SDRAM effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Low Power DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The X32 offering has two data strobes.

The 512Mb Low Power DDR SDRAM operates from a differential clock (CLK and /CLK); the crossing of CLK going HIGH and /CLK going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CLK.

Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access. The DLL signal that is typically used on standard DDR devices is not necessary on the Low Power DDR SDRAM. It has been omitted to save power.

The Low Power DDR SDRAM provides for programmable READ or WRITE burst lengths of 2,4,8 or 16. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of Low Power DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto-refresh mode is provided, along with a power saving power-down mode. Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial array self refresh, which allow users to achieve additional power saving. The temperature sensor is enabled by default and the partial array self refresh can be programmed through the extended mode register.

Features

- Functionality
  - Double-data-rate architecture; two data transfers per CLK cycle.
  - Bidirectional data strobe per byte data (DQS).
  - No DLL; CLK to DQS is not Synchronized.
  - Differential CLK inputs (CLK and /CLK).
  - Commands entered on each positive CLK edge.
  - DQS edge-aligned with data for Reads; center-aligned with data for Writes.
  - Four internal banks for concurrent operation.
  - Data masks (DM) for masking write data-one mask per byte.
  - Programmable burst lengths: 2, 4, 8, 16.
  - Programmable CAS Latency: 2, 3.
  - Concurrent auto pre-charge option is supported.
  - Auto refresh and self refresh modes.
  - Status read register (SRR)
  - LVCMOS-compatible inputs.
- Configuration
  - 16M X 32 (4M X 32 X 4Banks)
- Low Power Features
  - Low voltage power supply.
  - Auto TCSR (Temperature Compensated Self Refresh).
  - Partial Array Self Refresh power-saving mode.
  - Deep Power Down Mode.
  - Driver Strength Control.
- Operating temperature range:
  - Extended Test (ET): -25~85°C
  - Industrial (IT): -40~85°C
- Package
  - 90-Ball FBGA (8 X 13 X 0.8mm)

Notes:
1. Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the X32 is divided into four bytes. For the first byte (DQ0–DQ7) DM refers to DM0 and DQS refers to DQS0. For the second byte (DQ8–DQ15) DM refers to DM1 and DQS refers to DQS1. For the third byte(DQ16-DQ23) DM refers to DM2 and DQS refers to DQS2. And for the fourth byte(DQ24-DQ31) DM refers to DM3 and DQS refers to DQS3.
2. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

How to Order

Function	Density	IO Width	Pkg Type	Pkg Size	Speed & Latency	Option	INSIGNIS PART NUMBER:
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC166	Extended Test	NLD53PFJ-16ET
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC166	Industrial Temp	NLD53PFJ-16IT
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC200	Extended Test	NLD53PFJ-20ET
LPDDR	512Mb	X32	FBGA	8x13(x1.0)	PC200	Industrial Temp	NLD53PFJ-20IT

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Figure 1. Pin Configuration - FBGA-90 ball 0.8mm pitch (8mm x 13mm)

Top View

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ31	V_{SSQ}				V_{DDQ}	DQ16	V_{DD}
B	V_{DDQ}	DQ29	DQ30				DQ17	DQ18	V_{SSQ}
C	V_{SSQ}	DQ27	DQ28				DQ19	DQ20	V_{DDQ}
D	V_{DDQ}	DQ25	DQ26				DQ21	DQ22	V_{SSQ}
E	V_{SSQ}	DQS3	DQ24				DQ23	DQS2	V_{DDQ}
F	V_{DD}	DM3	NC				NC	DM2	V_{SS}
G	CKE	CK	/CK				/WE	/CAS	/RAS
H	A9	A11	A12				/CS	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	V_{SSQ}	DQS1	DQ8				DQ7	DQS0	V_{DDQ}
M	V_{DDQ}	DQ9	DQ10				DQ5	DQ6	V_{SSQ}
N	V_{SSQ}	DQ11	DQ12				DQ3	DQ4	V_{DDQ}
P	V_{DDQ}	DQ13	DQ14				DQ1	DQ2	V_{SSQ}
R	V_{SS}	DQ15	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}

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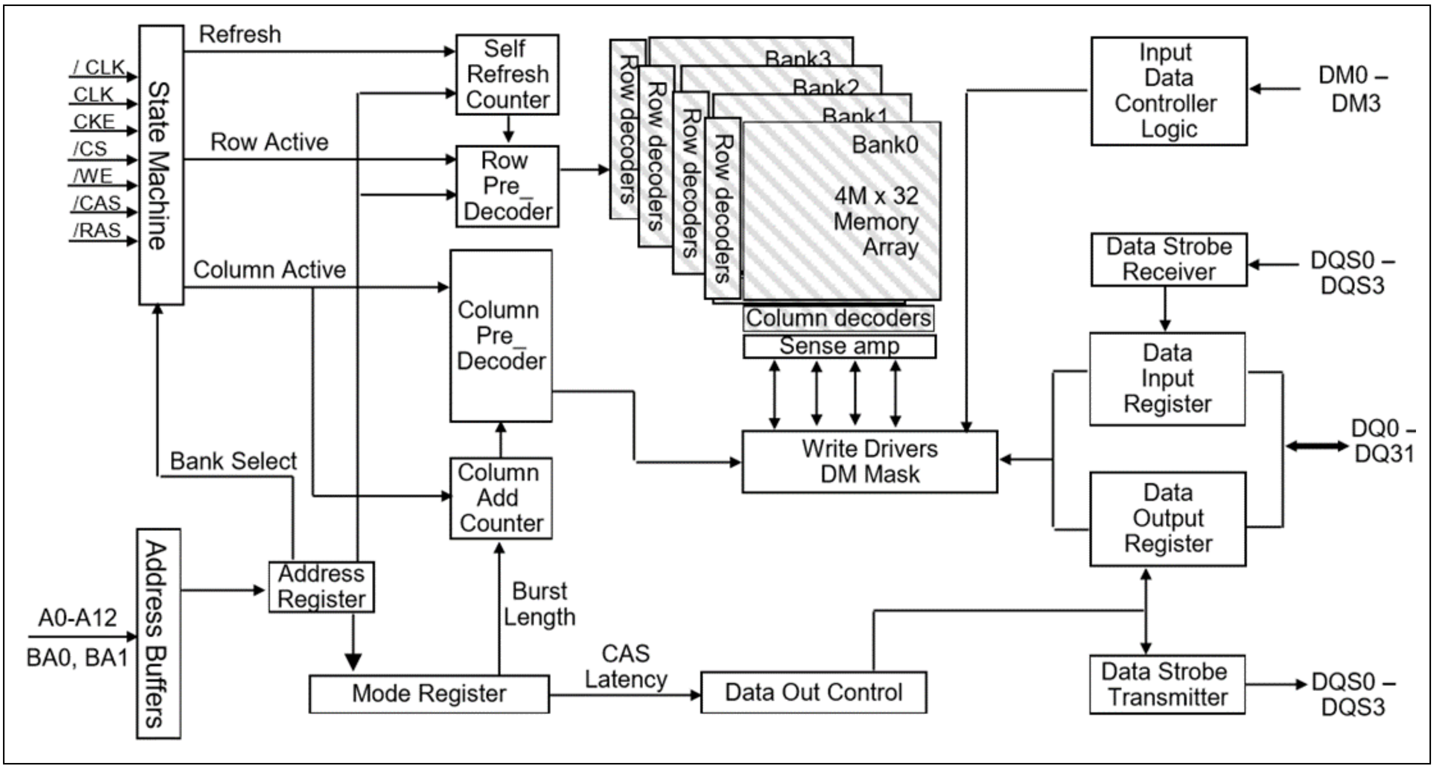
Figure 2. Block Diagram



Selection Guide

Device	Voltage		Clock Frequency	Access Time(t_{AC})		tRCD	tRP
	V_{DD}	V_{DDQ}		CL=2	CL=3		
NLD53PFJ	1.70-1.95V	1.70-V_{DD}	200MHz		5.0ns	15ns	15ns
			83MHz	6.0ns		15ns	15ns

Pin Descriptions

Table 1. Pin Descriptions

Symbol	Type	Description
CLK, /CLK	Input	Clock: CLK is the system clock input. CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of /CLK. Input and output data is referenced to the crossing of CLK and /CLK (both directions of the crossing).
CKE	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW allows PRECHARGE power-down and SELF REFRESH operations (all banks idle), or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions expect SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes.
/CS	Input	Chip select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	Command inputs: /RAS, /CAS, and /WE (along with /CS) define the command being entered.
DM0–DM3	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x32, DM0 corresponds to DQ0 – DQ7, DM1 corresponds to DQ8–DQ15, DM2 corresponds to DQ16-DQ23, and DM3 corresponds to DQ24-DQ31.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command.
A0-A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command. For 512Mb(X32), Row Address: A0 ~ A12, Column Address: A0 ~ A8.
DQ0-DQ32	I/O	Data input/output: Data bus for X32.
DQS0-DQS3	I/O	Data strobe: Output with read data, input with write data. DQS is edgealigned with read data, centered in write data. It is used to capture data. For the x32, DQS0 corresponds to DQ0 – DQ7, DQS1 corresponds to DQ8–DQ15, DQS2 corresponds to DQ16-DQ23, and DQS3 corresponds to DQ24-DQ31.
TQ	Output	Temperature sensor output: TQ High when LPDDR Tj exceeds 85℃. When TQ is 'High', self refresh is not supported.
VDDQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
VSSQ	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
VDD	Supply	Power Supply: Voltage dependent on option.
VSS	Supply	Ground.

Note: The signal may show up as a different symbol but it indicates the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb, /DQS = DQS# = $\overline{DQS}$ = DQSb

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Functional Description

The 512Mb Low Power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits.

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Read and write accesses to the Low Power DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command.

The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL signal that is typically used on standard DDR devices is not necessary on the Low Power DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Low Power DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

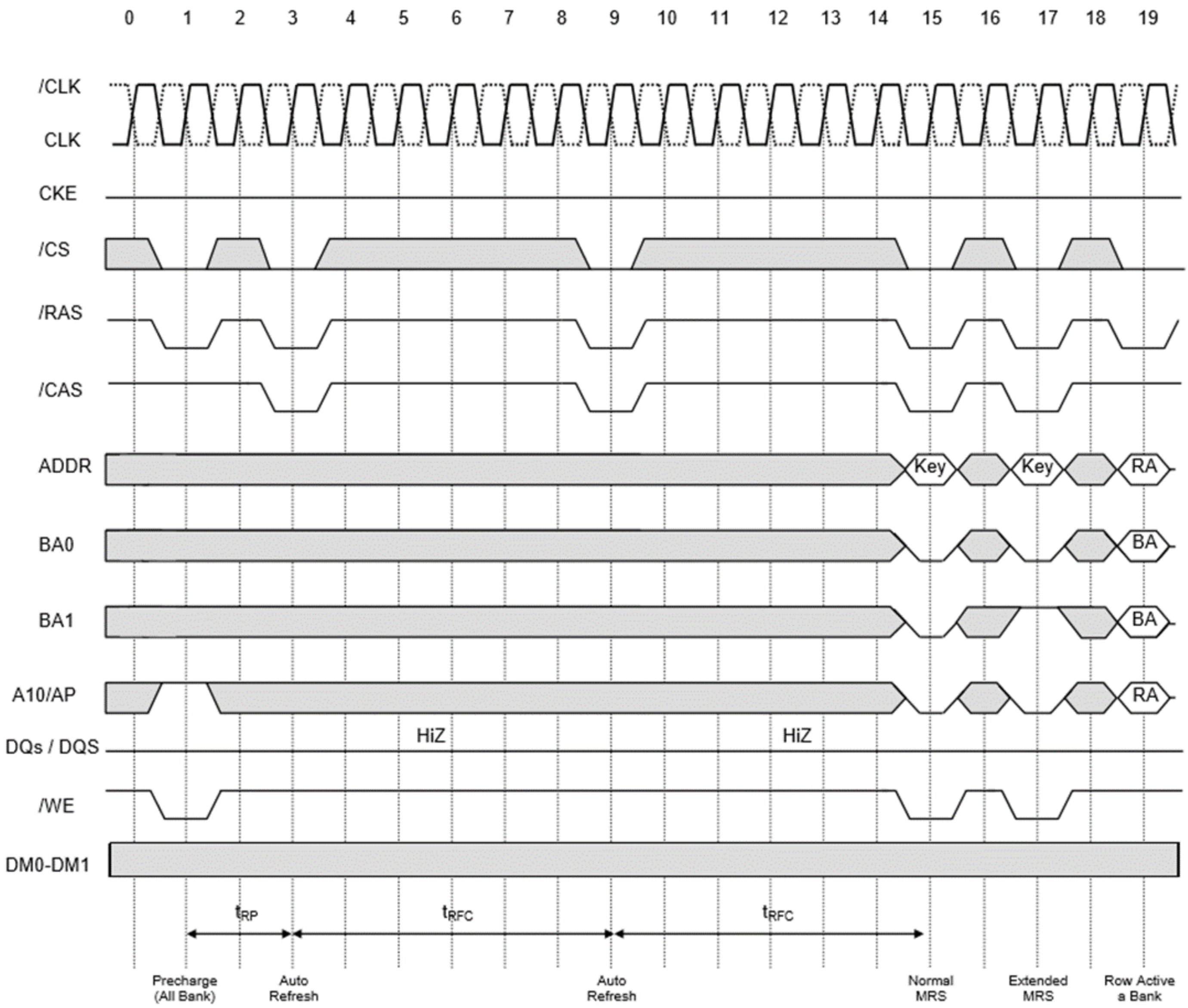
Low Power DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Low Power DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Low Power DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended the core power (VDD) and I/O power (VDDQ) be from the same power source and brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200µs (minimum) delay is required by the Low Power DDR SDRAM prior to applying an executable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. As part of the individualization sequence, two AUTO REFRESH commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued between steps 10 and 11.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least tMRD time.
11. The Low Power DDR SDRAM has been properly initialized and is ready to receive any valid command.

Figure 3. Initialize and Load Mode Register[1,2,3]



Notes:

1. The two AUTO REFRESH commands at T3 and T9 may be applied before either LOAD MODE REGISTER (LMR) command.
2. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address
3. The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order; However, all must occur prior to an Active command.
4. NOP or DESELECT commands are required for at least 200μs.
5. Other valid commands are possible.
6. NOPs or DESELECTs are required during this time.

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Register Definition

Mode Registers
The mode registers are used to define the specific mode of operation of the Low Power DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all Low Power DDR SDRAM devices, and the extended mode register, which exists on all Low Power DDR SDRAM devices.

Standard Mode Register
The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Table 1 on page 10. The standard mode register is programmed via the LOAD MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again. Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0–A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4–A6 specify the CAS latency, and A7–A12 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length
Read and write accesses to the Low Power DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Table 2. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2,4,8 or 16 are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap until a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, by A3–Ai when BL = 8, by A4–Ai when BL=16 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

The programmed burst length applies to both READ and WRITE bursts.

Burst Type
Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See the Burst Definition Table below for more information.

READ Latency
The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in Table 1 on page 10. For CL = 3, if the READ command is registered at clock edge n, then the data will nominally be available at (2 clocks + tAC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally available at (1 clock + tAC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 2. Standard Mode Register Definition

M14-BA1	M13-BA0	M12-A12	M11-A11	M10-A10	M9-A9	M8-A8	M7-A7	M6-A6	M5-A5	M4-A4	M3-A3	M2-A2	M1-A1	M0-A0
0	0	Operation Mode						CAS Latency			BT	Burst Length		

M14	M13	Mode Register Definition
0	**0**	**Standard Mode Register**
0	1	Status Read Register
1	0	Extended Mode Register
1	1	Reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M12	M11	M10	M9	M8	M7		Operating Mode
0	0	0	0	0	0	Valid	Normal Operation
-	-	-	-	-	-	-	All other states reserved

M3	Burst Type
0	Sequential
1	Interleaved

Table 3. Burst Definition

Burst Length	Starting Column Address				Order of Accesses Within a Burst	
					Type = Sequential	Type = Interleaved
2				A0		
				0	0-1	0-1
				1	1-0	1-0
4			A1	A0		
			0	0	0-1-2-3	0-1-2-3
			0	1	1-2-3-0	1-0-3-2
			1	0	2-3-0-1	2-3-0-1
			1	1	3-0-1-2	3-2-1-0
8		A2	A1	A0		
		0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
		0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
		0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
		0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
		1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
		1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
		1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
		1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
16	A3	A2	A1	A0		
	0	0	0	0	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
	0	0	0	1	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-0-3-2-5-4-7-6-9-8-11-10-13-12-15-14
	0	0	1	0	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-0-1-6-7-4-5-10-11-8-9-14-15-12-13
	0	0	1	1	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-2-1-0-7-6-5-4-11-10-9-8-15-14-13-12
	0	1	0	0	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-0-1-2-3-12-13-14-15-8-9-10-11
	0	1	0	1	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-4-7-6-1-0-3-2-13-12-15-14-9-8-11-10
	0	1	1	0	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-4-5-2-3-0-1-14-15-12-13-10-11-8-9
	0	1	1	1	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-15-14-13-12-11-10-9-8
	1	0	0	0	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7	8-9-10-11-12-13-14-15-0-1-2-3-4-5-6-7
	1	0	0	1	9-10-11-12-13-14-15-0-1-2-3-4-5-6-7-8	9-8-11-10-13-12-15-14-1-0-3-2-5-4-7-6
	1	0	1	0	10-11-12-13-14-15-0-1-2-3-4-5-6-7-8-9	10-11-8-9-14-15-12-13-2-3-0-1-6-7-4-5
	1	0	1	1	11-12-13-14-15-0-1-2-3-4-5-6-7-8-9-10	11-10-9-8-15-14-13-12-3-2-1-0-7-6-5-4
	1	1	0	0	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-8-9-10-11-4-5-6-7-0-1-2-3
	1	1	0	1	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-12-15-14-9-8-11-10-5-4-7-6-1-0-3-2
	1	1	1	0	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-12-13-10-11-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-14-13-12-11-10-9-8-7-6-5-4-3-2-1-0

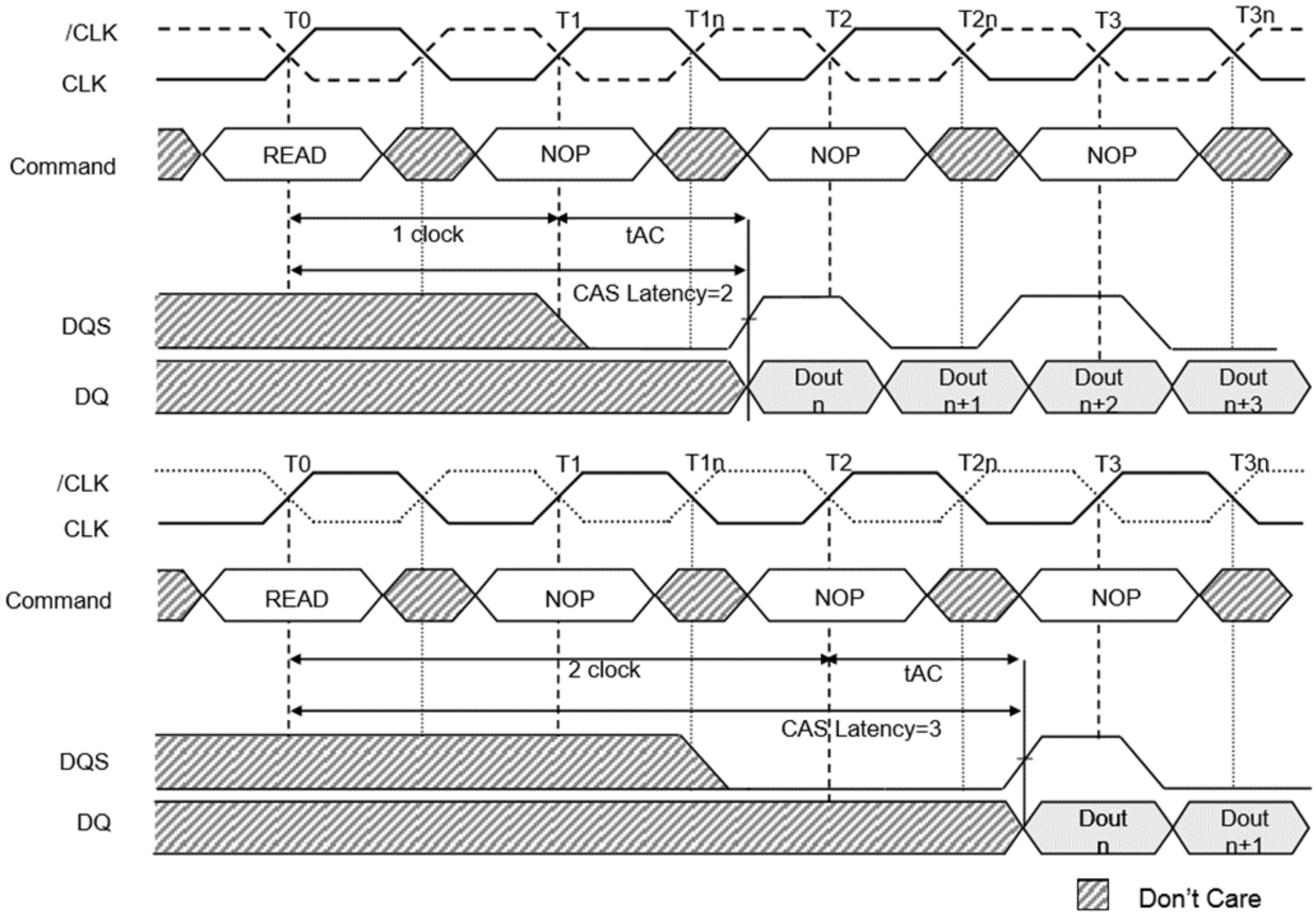
Notes:

1. For BL = 2, A1–A*i* select the two-data-element block; A0 selects the first access within the block.
2. For BL = 4, A2–A*i* select the four-data-element block; A0–A1 select the first access within the block.
3. For BL = 8, A3–A*i* select the eight-data-element block; A0–A2 select the first access within the block.
4. For BL=16, A4–A*i* select the sixteen-data-element block; A0–A3 select the first access within the block.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. A*i* = the most significant column address bit for a given configuration.

Table 4. CAS Latency

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 3
-5I (200)	f ≤83	f ≤200

Figure 4. CAS Latency



Notes:
1. BL = 4 in the cases shown.
2. Shown with nominal tAC and nominal tDQSCLK

Operating Mode
The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7– A12 each set to zero, and bits A0–A6 set to the desired values. All other combinations of values for A7–A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register
The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh. This device has default values for the extended mode register (if not programmed, the device will operate with the default values – PASR = Full Array, DS = Full Drive).

Temperature Compensated Self Refresh
A temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh
For further power savings during SELF REFRESH, the PASR feature allows the controller to select the mount of memory that will be refreshed during SELF REFRESH. The refresh options are as follows:

- Full array: banks 0, 1, 2, and 3
- Half array: banks 0 & 1
- Quarter array: bank 0
- One Eighth array: Half of Bank0
- One Sixteenth array: Quarter of Bank0

WRITE and READ commands can still occur during standard operation, but only the selected banks will be refreshed during SELF REFRESH. Data in banks that are disabled will be lost.

Output Driver Strength
Because the Low Power DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 ~ A7 of the extended mode register can be used to select the driver strength of the DQ outputs. There are five allowable settings for the output drivers.

Table 5. Extended Mode Register Table[1,2]

EM14-BA1	EM13-BA0	EM12-A12	EM11-A11	EM10-A10	EM9-A9	EM8-A8	EM6-A7	EM6-A6	EM5-A5	EM4-A4	EM3-A3	EM2-A2	EM1-A1	EM0-A0
1	0	All must be set to '0'					Driver Strength			0	0	PASR		

EM14	EM13	Mode Register Definition
0	0	Standard Mode Register
0	1	Status Read Register
1	**0**	**Extended Mode Register**
1	1	Reserved

EM2	EM1	EM0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank(BA1=0)
0	1	0	Quarter of Total Bank(BA1=BA0=0)
0	1	1	RFU
1	0	0	RFU
1	0	1	One Eighth of Total Bank (BA1=BA0=Row Address MSB=0)
1	1	0	One Sixteenth of Total Bank (BA1=BA0=Row Address2 MSBs=0)
1	1	1	RFU

EM7	EM6	EM5	Driver Strength
0	0	0	100%
0	0	1	50%
0	1	0	25%
0	1	1	12.5%
1	0	0	75%
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes:
1. EM14 and EM13 (BA1 and BA0) must be "1, 0" to select the Extended Mode Register (vs. the base Mode Register).
2. RFU: Reserved for Future Use

Status Read Registers

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the device, as shown in Table 5 (page 13). The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

- The device must be properly initialized and in the idle or all banks precharged state.
- Issue a LOAD MODE REGISTER command with BA[1:0] = 01 and all address pins set to 0.
- Wait tSRR; only NOP or DESELECT commands are supported during the tSRR time.
- Issue a READ command.
- Subsequent commands to the device must be issued tSRC after the SRR READ command is issued; only NOP or DESELECT commands are supported during tSRC.

SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first bit of the burst, with the output being "Don't Care" on the second bit of the burst.

Table 6. Status Register Table

S31~S16[1]	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Reserved	Density			Type	Width	Refresh Rate			Revision ID				Manufacturer ID			

S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

S12	Device Type
0	LPDDR
1	Reserve

S11	Device Width
0	16 bits
1	32 bits

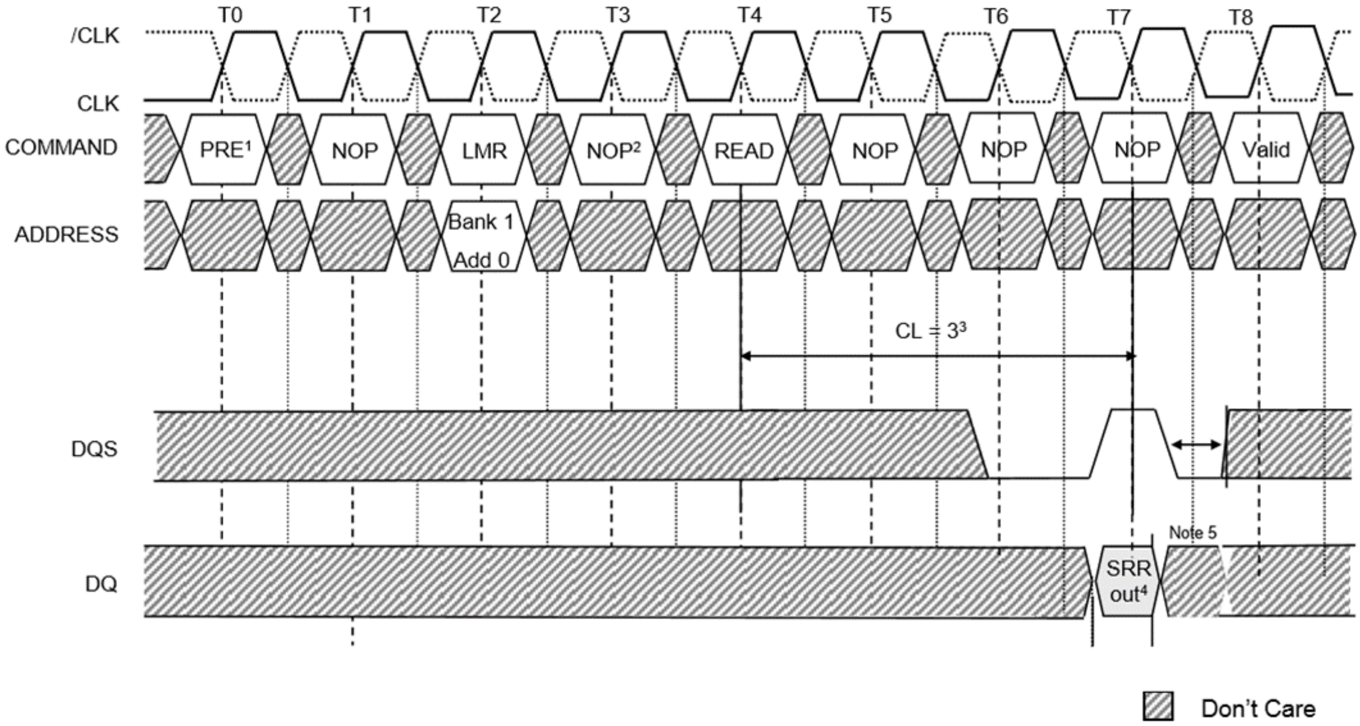
S10	S9	S8	Refresh Multiplier[2]
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	2X
1	0	0	1X
1	0	1	Reserved
1	1	0	0.25X
1	1	1	Reserved

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Fidelix
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer's revision number starts at '0000' and increments by '0001' each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
~				
1	1	1	1	

Notes:
1. Reserved bits should be set to 0 for future compatibility.
2. Refresh multiplier is based on the device on-board temperature sensor.
   Requited periodic refresh interval = tREFI X multiplier.
   Self refresh is not supported for automotive device at high temperature. (85°C to 105°C)

Figure 5. Status Read Register Timing



Notes:
1. All banks must be idle prior to status register read.
2. NOP or DESELECT commands are required between the LMR and READ commands(tSRR), and between the READ and the next VALID command (tSRC).
3. CAS latency is predetermined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a “Don't Care.”

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the Low Power DDR SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency, when the data transfers require a different rate of speed.
2. Stopping the clock altogether.

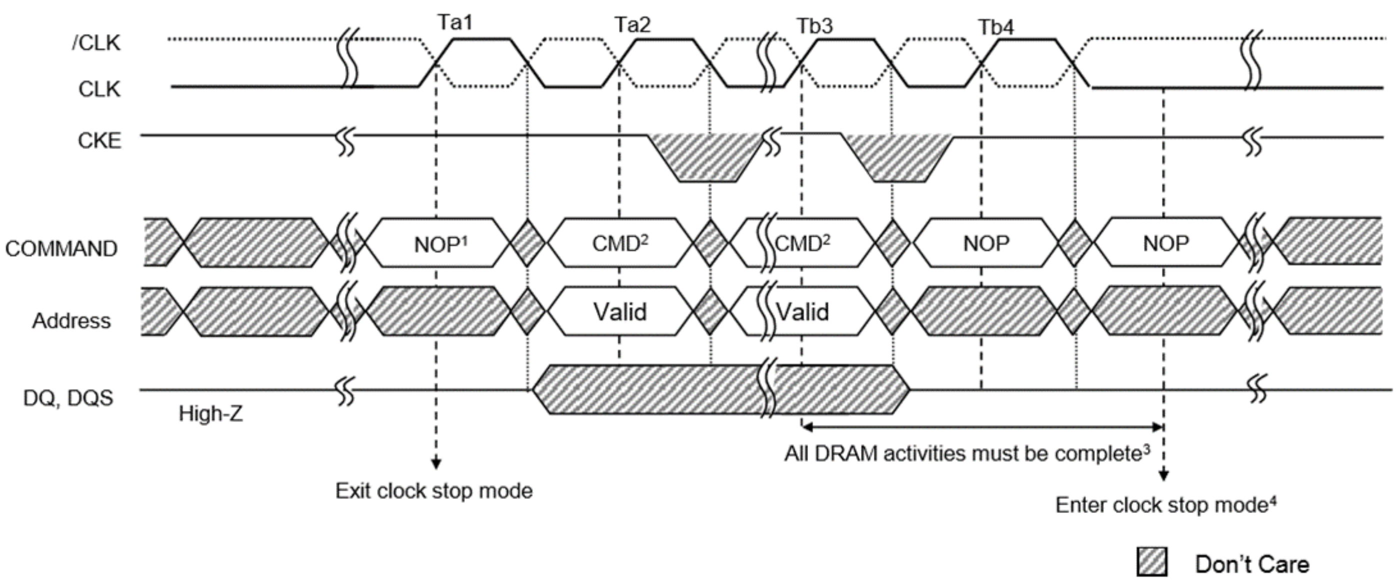
Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Low Power DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped all together, if there are no data accesses in progress, either WRITEs or READs that would be affected by this change; i.e., if a WRITE or a READ is in progress the entire data burst must be through the pipeline prior to stopping the clock. CKE must be held HIGH with CLK = LOW and /CLK = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued. Figure 6 illustrates the clock stop mode.

It is recommended that the Low Power DDR SDRAM should be in a precharged state if any changes to the clock frequency are expected. This will eliminate timing violations that may otherwise occur during normal operational accesses.

Figure 6. Clock Stop Mode



Notes:
1. Prior to Ta1 the device is in clock stop mode. To exit, at least one NOP is required before any valid command.
2. Any valid command is allowed, device is not in clock suspend mode.
3. Any DRAM operation already in process must be completed before entering clock stop mode. This includes tRCD, tRP, tRFC, tMRD, tWR, all data-out for READ bursts. This means the DRAM must be either in the idle or precharge state before clock suspend mode can be entered.
4. To enter and maintain a clock stop mode: CLK = LOW, /CLK = HIGH, CKE = HIGH.

Commands

The tables below provide quick references of available commands. This is followed by a written description of each command. Three additional Truth Tables provide CKE commands and current/ next state information.

Table 7. Truth Table – Commands

Note: 1 and 11 apply to all commands

Name (Function)	/CS	/RAS	/CAS	/WE	ADDR	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8, 10
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER (standard or extended mode registers)	L	L	L	L	Op-Code2	2
Deep Power Down (Enter DPD Mode)	L	H	H	L	Op-Code2	11

Notes:

1. CKE is HIGH for all commands shown except SELF REFRESH and Deep Power Down.
2. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12 provide the op- code to be written to the selected mode register.
3. BA0–BA1 provide bank address and A0–A12 provide row address.
4. BA0–BA1 provide bank address; A0–A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
9. DESELECT and NOP are functionally interchangeable.
10. This command is a BURST TERMINATE if CKE is HIGH.
11. This command is a Deep Power Down if CKE is Low.
12. All states and sequences not shown are reserved and/or illegal.

Table 8. Truth Table – DM Operation

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

Note: Used to mask write data; provided coincident with corresponding data.

DESELECT

The DESELECT function (/CS HIGH) prevents new commands from being executed by the Low Power DDR SDRAM. The Low Power DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (/CS = LOW, /RAS = /CAS = /WE = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER
The mode registers are loaded via inputs A0–A12. See mode register descriptions in “Register Definition” on page 8. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE
The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ
The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE
The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE
The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge
Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS (MIN), as described for each burst type in “Operations” on page 24. The user must not issue another command to the same bank until the precharge time (tRP) is completed.

BURST TERMINATE
The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in “Operations” on page 24. The open page which the READ burst was terminated from remains open.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the Low Power DDR SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 512Mb Low Power DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125μs (maximum). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends tRFC later.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the Low Power DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Low Power DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting). For a full array refresh, all four banks are refreshed simultaneously with the refresh frequency set by an internal self refresh oscillator. This oscillator changes due to the temperature sensors input. As the case temperature of the Low Power DDR SDRAM increases, the oscillation frequency will change to accommodate the change of temperature. This happens because the DRAM capacitors lose charge faster at higher temperatures. To ensure efficient power dissipation during self refresh, the oscillator will change to refresh at the slowest rate possible to maintain the devices data.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Low Power DDR SDRAM must have NOP commands issued for tXSR is required for the completion of any internal refresh in progress. Self refresh is not supported for automotive devices at high temperature (85°C to 105°C).

DEEP POWER DOWN

Deep Power Down Mode is an operating mode to achieve extreme power reduction by cutting the power of the whole memory array of the device. Data will not be retained once the device enters DPD Mode. Full initialization is required when the device exits from DPD Mode.

Maximum Ratings

Voltage on V_{DD}/V_{DDQ} Supply Relative to V_{SS}	-0.5V to +3.6V
Voltage on Inputs, NC or I/O Pins Relative to V_{SS}	-0.5V to +3.6V
Storage Temperature (plastic)	-55°C to + 150°C
Power Dissipation	1W

*Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9. Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
NLD53PFJ-xxET	Extended Test	-25℃ to +85℃	1.7V ~ 1.95V	1.7V ~ V_{DD}
NLD53PFJ-xxIT	Industrial	-40℃ to +85℃		

Table 10. DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS [1,2]

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	1.7	1.95	V
I/O Supply Voltage	V_{DDQ}	1.7	V_{DD}	V
Input High Voltage: Logic 1 All Inputs [3.]	V_{IH}	0.7* V_{DDQ}	V_{DDQ} +0.3	V
Input Low Voltage: Logic 0 All Inputs [3.]	V_{IL}	-0.3	0.3*V_{DDQ}	V
Data Output High Voltage: Logic 1: All Inputs(-0.1mA)	V_{OH}	0.9* V_{DDQ}		V
Data Output Low Voltage: Logic 0: All Inputs(0.1mA)	V_{OL}		0.1* V_{DDQ}	V
Input Leakage Current: Any Input 0V=V_{IN}=V_{DD} (All other pins not under test=0V)	II	-5	5	㎂
Output Leakage Current: DQs are disabled; 0V= V_{OUT}=V_{DDQ}	I_{OZ}	-5	5	㎂

Table 11. AC Operating Conditions [1,2,3,4,5,6]

Parameter / Condition	Value	Units
AC input levels (Vih / Vil)	0.8 x VDDQ / 0.2 x VDDQ	V
Input timing measurement reference level	0.5 x VDDQ	V
Input signal minimum slew rate	1.0	V/ns
Output timing measurement reference level	0.5 x VDDQ	V
Output load condition	AC Output Load Circuit on page 19	V

Notes:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-40°C ≤ TA ≤ +85°C for IT parts) is ensured.
2. An initial pause of 200µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
3. All states and sequences not shown are illegal or reserved.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet t_{OH} before going High-Z.
6. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to V_{IH}//2 = crossover point. If the input transition time is longer than t_T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the V_{IH}/2 crossover point.

Table 12. IDD Specifications and Conditions

Parameter/Condition		Symbol	Max -5I (200)	Units	Notes
Operating one bank active precharge current: tRC = tRC(MIN); tCLK = tCLK(MIN); CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD0	70	mA	1, 6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2P	300	µA	2, 4
Precharge power-down standby current with CLK stopped: All banks idle; CKE is LOW, CS is HIGH; CLK = LOW, /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2PS	300	µA	2, 4
Precharge non power-down standby current: All banks idle; CKE = HIGH; CS = HIGH; tCLK =tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2N	15	mA	5
Precharge non power-down standby current: CLK stopped; All banks idle; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD2NS	8	mA	5
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3P	3	mA	2, 4
Active power-down standby current: CLK stopped; One bank active; CKE = LOW; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3PS	2	mA	2, 4
Active non power-down standby: One bank active; CKE = HIGH; CS = HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two cycles; Data bus inputs are stable.		IDD3N	15	mA	1
Active non-power-down standby: CLK stopped; One bank active; CKE = HIGH; CS = HIGH; CLK = LOW; /CLK = HIGH; Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.		IDD3NS	8	mA	1
Operating burst read: One bank active; BL = 4; tCLK = tCLK(MIN); Continuous READ bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4R	115	mA	1, 6
Operating burst write: One bank active; BL = 4; tCLK = tCLK(MIN); Continuous WRITE bursts; Address inputs are switching; 50 percent data changing each burst.		IDD4W	115	mA	1, 6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable.	tRC = tRFC(138ns)	IDD5	95	mA	7
Precharge power-down standby current: All banks idle, CKE is LOW; CS is HIGH; tCLK = tCLK(MIN); Address and control inputs are switching every two CLK cycles; Data bus inputs are stable.	tRC = 7.8125µs	IDD5a	3	mA	3, 7
Self refresh: CKE = LOW; tCLK = tCLK(MIN); Address and control inputs are stable; Data bus inputs are Stable.	Full Array, 85°C	IDD6a	600	µA	8, 9
	Full Array, 45°C	IDD6a	450	µA	8, 9
	Half Array, 85°C	IDD6b	500	µA	8, 9
	¼ Array, 85°C	IDD6c	400	µA	8, 9
Deep Power Down Current; Address, control and data bus inputs are STABLE		IDD7	10	µA	10

Notes:

1. MIN (tRC or tRFC) for IDD measurements is the smallest multiple of tCLK that meets the minimum absolute value for the respective parameter. tRAS (MAX) for IDD measurements is the largest multiple of tCLK that meets the maximum absolute value for tRAS.
2. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs.
3. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (tRFC [MIN]) else CKE is LOW (i.e., during standby).
4. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/ DM/DQS slew rate is less than 0.5V/ns, timing must be derated: ***50ps (pending) must be added to tDS and tDH for each 100mv/ns reduction in slew rate***. If slew rate exceeds 4V/ns, functionality is uncertain.
5. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
6. Switching is defined as:
   - address and command: inputs changing between HIGH and LOW once per two clock cycles;
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

7. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
8. With the inclusion of the temperature sensor on the low-power DDR device, these numbers are shown as examples only, and will change due to the junction temperature that the device is sensing. They are expected to be maximum values at this time.
9. Enables on-chip refresh and address counters.
10. Device must be in the all banks idle state prior to entering Deep Power Down.

Table 13. Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance (A0-A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE)	CIN1	1.5	3.0	pF
Input capacitance (CLK, /CLK)	CIN2	1.5	3.0	pF
Data & DQS input / output capacitance	COUT	3.0	5.0	pF
Input capacitance (DM)	CIN3	3.0	5.0	pF

AC Output Load Circuit

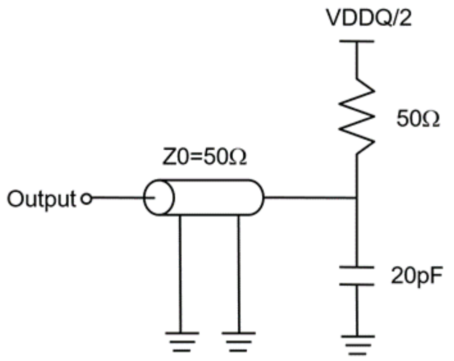


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Table 14. Electrical Characteristics and Recommended AC Operating Conditions

AC Characteristics		Symbol	-5I (200)		Units	Notes
Parameter			Min	Max		
Access window of DQ from CLK & /CLK	CL=3	tAC(3)	2.0	5.0	ns	
	CL=2	tAC(2)	2.0	6.0		
CLK high-level width		tCH	0.45	0.55	tCLK	
CLK low-level width		tCL	0.45	0.55	tCLK	
System Clock cycle time	CL=3	tCLK(3)	5	100	ns	1
	CL=2	tCLK(2)	12	-	ns	
Auto precharge write recovery + precharge time		tDAL	5	-	tCLK	16
DQ and DM input hold time relative to DQS		tDH	0.48	-	ns	9, 13, 15
DQ and DM input setup time relative to DQS		tDS	0.48	-	ns	17
DQ and DM input pulse width (for each input)		tDIPW	1.6	-	ns	
Access window of DQS from CLK & /CLK		tDQSCLK	2.0	5.0	ns	
DQS input high-pulse width		tDQSH	0.4	0.6	tCLK	
DQS input low-pulse width		tDQSL	0.4	0.6	tCLK	
Data strobe edge to Dout edge		tDQSQ	-	0.4	ns	8, 9
WRITE command to first DQS latching transition		tDQSS	0.75	1.25	tCLK	
DQS falling edge to CLK rising – setup time		tDSS	0.2	-	tCLK	
DQS falling edge from CLK rising – hold time		tDSH	0.2	-	tCLK	
Half-CLK period		tHP	tCH, tCL	-	ns	12
Data-out High-Z window from CLK & /CLK		tHZ	-	5.0	ns	3, 11
Data-out Low-Z window from CLK & /CLK		tLZ	1.0	-	ns	3, 11
Transition Time		t_T	0.5	1.2	ns	
Address and control input hold time		tIH	0.9	-	ns	2, 15
Address and control input setup time		tIS	0.9	-	ns	2, 15
Address and control input pulse width		tIPW	2.2	-	ns	17
LOAD MODE REGISTER command cycle time		tMRD	2	-	tCLK	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		tQH	tHP -tQHS	-	ns	8, 9
Data hold skew factor		tQHS	-	0.5	ns	
ACTIVE-to-PRECHARGE command		tRAS	42	70,000	ns	10
ACTIVE-to-ACTIVE command period		tRC	55	-	ns	
AUTO REFRESH command period		tRFC	80	-	ns	14
ACTIVE-to-READ or WRITE delay		tRCD	15	-	ns	
PRECHARGE command period		tRP	15	-	ns	
DQS read preamble	CL=3	tRPRE(3)	0.9	1.1	tCLK	11
	CL=2	tRPRE(2)	0.5	1.1	tCLK	11
DQS read postamble		tRPST	0.4	0.6	tCLK	
Read of SRR to next valid command		tSRC	CL+1	-	tCLK	
SRR to Read		tSRR	2	-	tCLK	
Internal temperature sensor valid temperature output enable		tTQ	2	-	ms	
ACTIVE bank *a* to ACTIVE bank *b* Delay		tRRD	10	-	ns	

Table 15. Electrical Characteristics and Recommended AC Operating Conditions (continued)

AC Characteristics	Symbol	-5I (200)		Units	Notes
Parameter		Min	Max		
DQS write preamble	tWPRE	0.25	-	tCLK	
DQS write preamble setup time	tWPRES	0	-	ns	5, 6
DQS write postamble	tWPST	0.4	0.6	tCLK	4
Write recovery time	tWR	15	-	ns	
Internal WRITE to READ command delay	tWTR	2	-	tCLK	
Average periodic refresh interval	tREFI	-	7.8	μs	7
Exit SELF REFRESH to first valid command	tXSR	120	-	ns	18
Exit power-down mode to first valid command	tPDX	25	-	ns	19
Minimum tCKE HIGH/LOW time	tCKE	1	-	tCLK	

Notes

1. CAS latency definition: for CL = 2, the first data element is valid at (tCLK + tAC) after the CLK at which the READ command was registered; for CL = 3, the first data element is valid at (2 × tCLK + tAC) after the first CLK at which the READ command was registered.
2. Fast command/address input slew rate ≥ 1V/ns. Slow command/address input slew rate ≥ 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: ***tIS has an additional 50ps (pending) per each 100mV/ns*** reduction in slew rate from the 0.5V/ns. ***tIH has 0ps added (pending);*** that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
6. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command.
7. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125μs.
8. The valid data window is derived by achieving other specifications: tHP (tCLK/2), tDQSQ, and tQH (tHP - tQHS). The data valid window derates directly proportional with the CLK duty cycle and a practical data valid window can be derived. The CLK is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
9. Referenced to each output group: DQS0 with DQ0–DQ7; and DQ1 with DQ8–DQ1
10. READs and WRITEs with auto precharge are allowed to be issued before tRAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
11. tHZ (MAX) will prevail over tDQSCLK (MAX) + tRPST (MAX) condition.
12. tHP (MIN) is the lesser of tCL minimum and tCH minimum actually applied to the device CLK and /CLK inputs, collectively.
13. Random addressing changing 50 percent of data changing at every transfer.
14. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising CLK edge, until tRFC later.
15. The transition time for input signals (/CAS, CKE, /CS, DM, DQ, DQS, /RAS, /WE, and addresses) are measured between VIL(DC) to VIH(AC) for rising input signals and VIH(DC) to VIL(AC) for falling input signals.
16. tDAL = (tWR/tCLK) + (tRP/tCLK): for each term, if not already an integer, round to the next higher integer.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. CLK must be toggled a minimum of two times during this period.
19. CLK must be toggled a minimum of one time during this period.
20. This device can support 45/55 of duty rate for tDQSCLK in case of 50/50 of CLK input.

Operations

Bank/row Activation

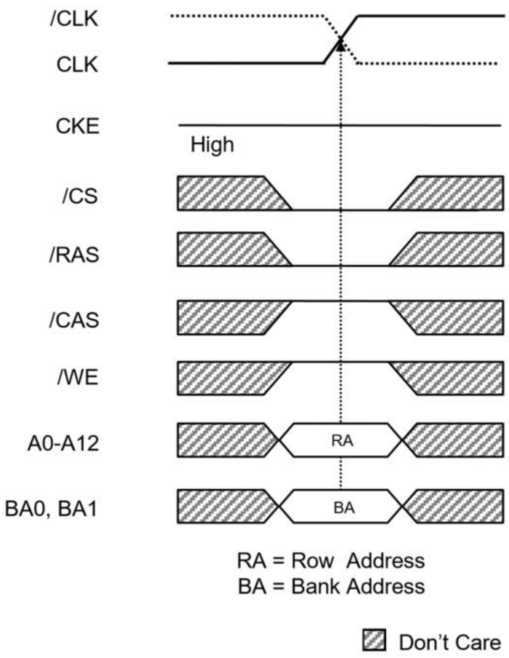
Before any READ or WRITE commands can be issued to a bank within the Low Power DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 7.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 18ns with a 133 MHz clock (7.5ns period) results in 2.4 clocks rounded to 3.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure 7. Activating a Specific Row in a Specific Bank



READ
READ bursts are initiated with a READ command, as shown in Figure 8.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CLK and /CLK). Figure 9 shows general timing for each possible CAS latency setting. DQS is driven by the Low Power DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of tDQSCLK (DQS transition skew to CLK) and tAC (data-out transition skew to CLK) is depicted in Figure 30.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued ***x*** cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). This is shown in Figure 10.

A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 11. Full speed random read accesses within a page (or pages) can be performed as shown in Figure 12.

Figure 8. READ Command

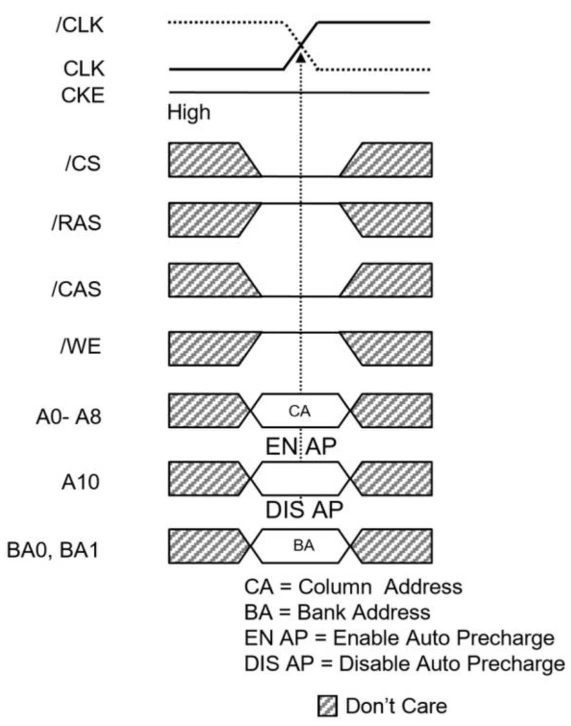


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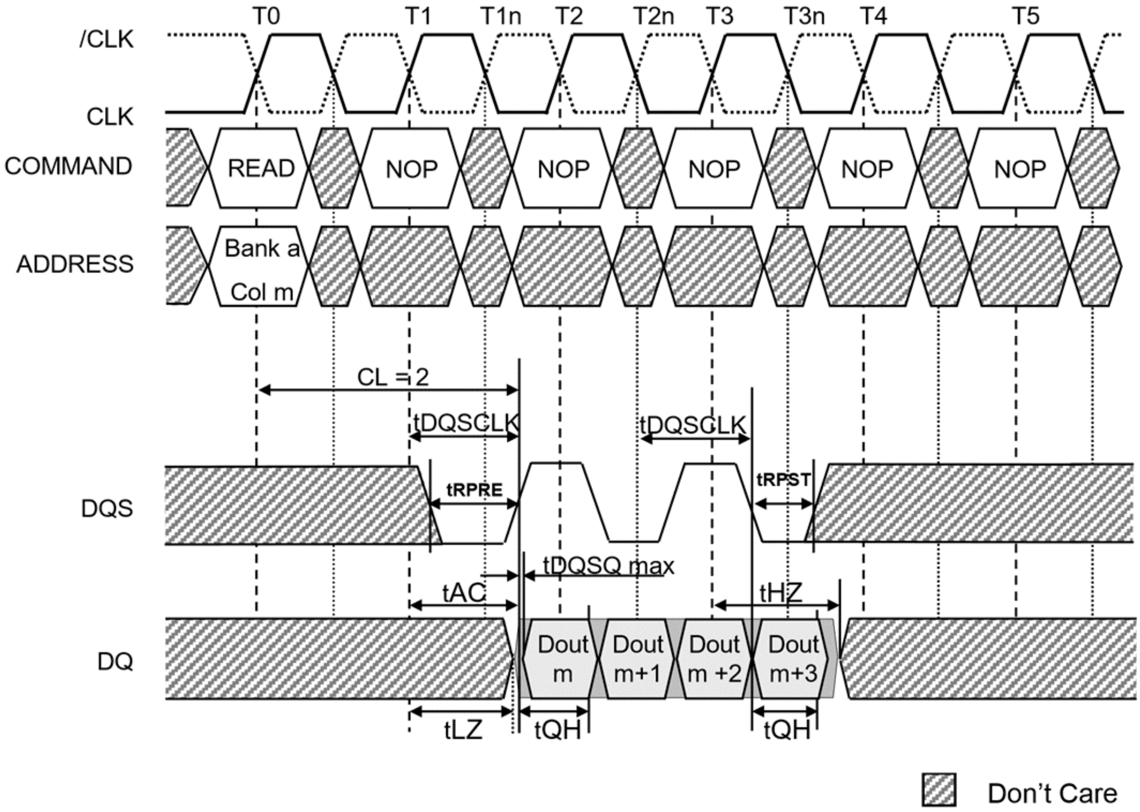
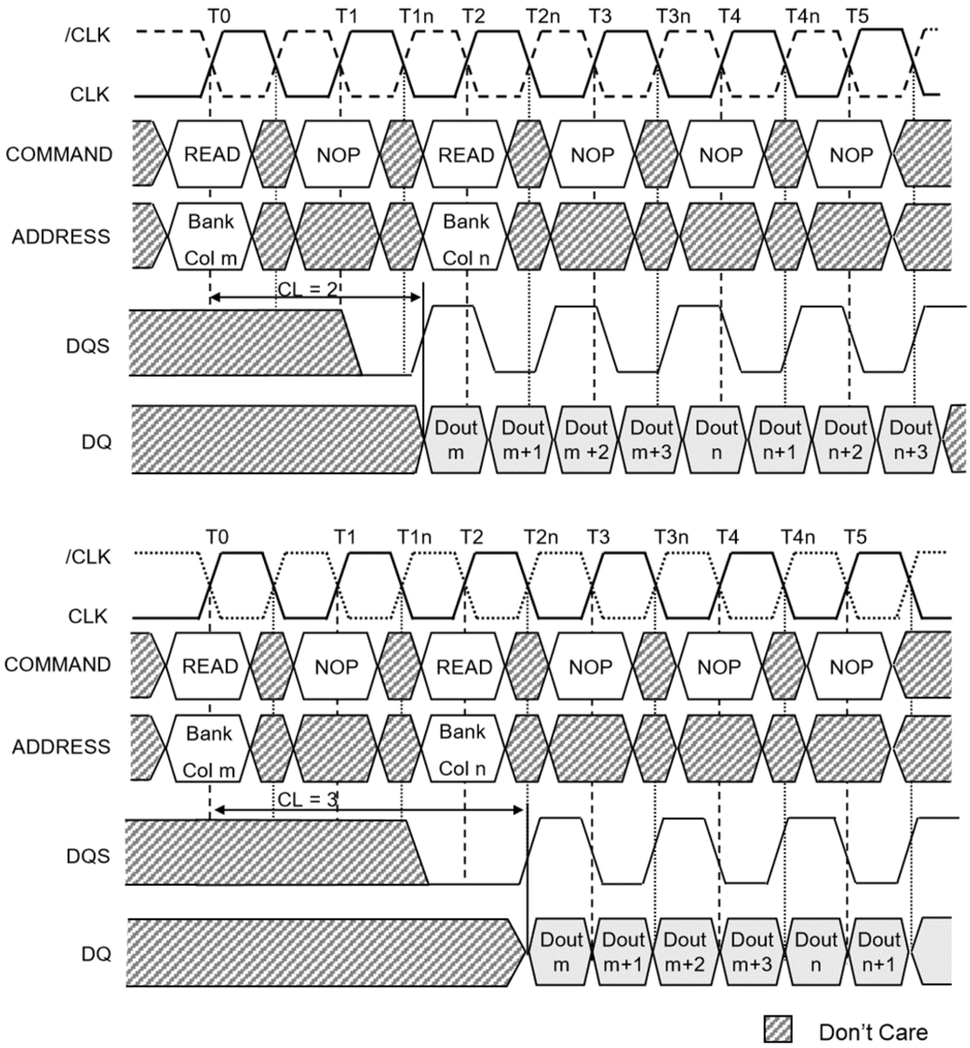
Figure 9. READ Operation



Notes:
1. Dout m = data-out from column m. 2.
2. BL = 4.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.

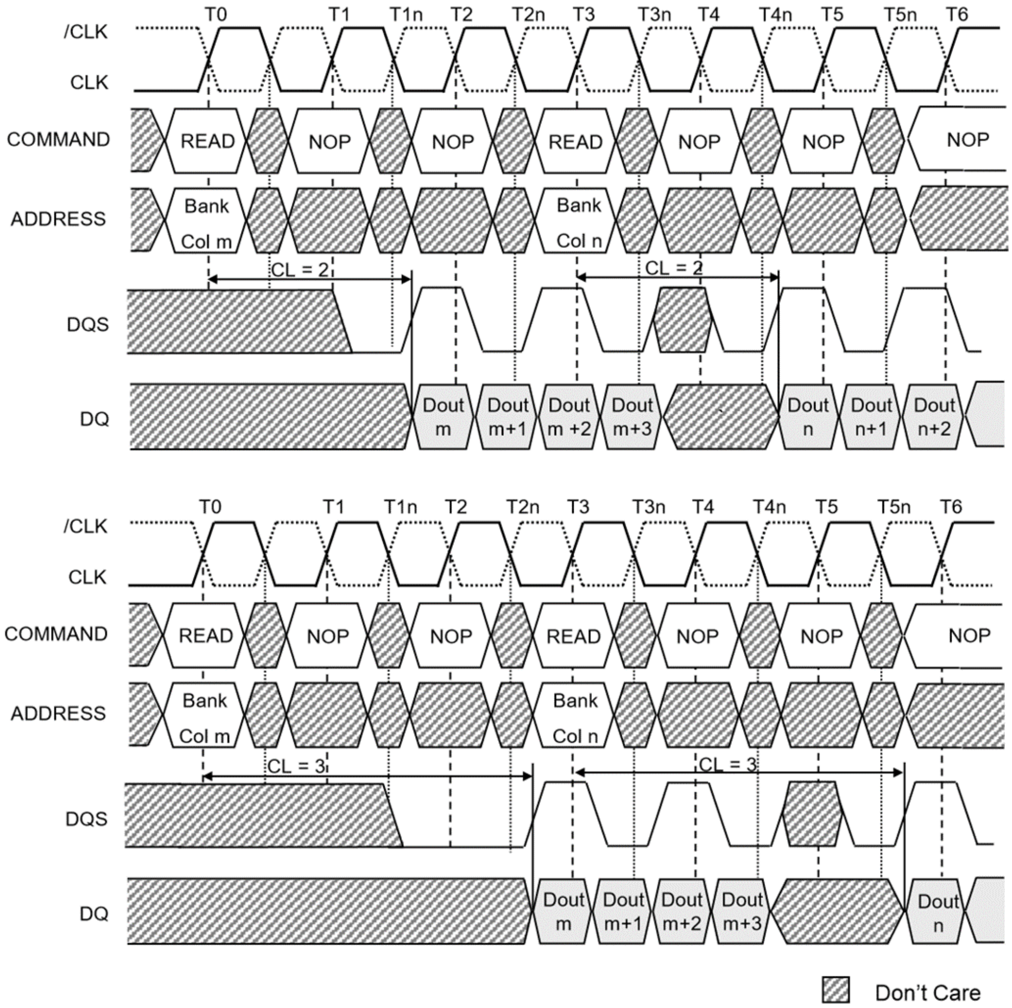
Figure 10. Consecutive Read Bursts



Notes:

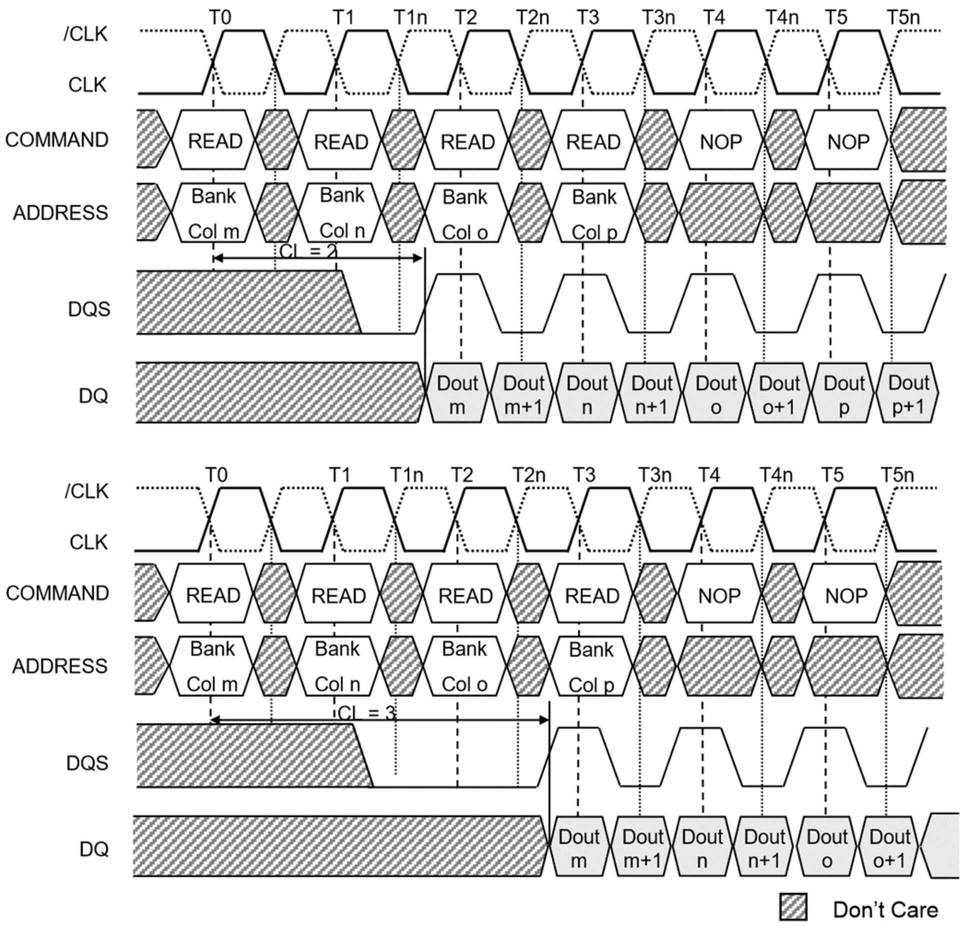
1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents consecutive READ commands issued to the device.

Figure 11. Read-to-Read Operation



Notes:
1. Dout m (or n) = data-out from column m (or column n).
2. BL = 4 in the cases shown
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. This example represents nonconsecutive READ commands issued to the device.

Figure 12. Random READ Accesses



Notes:
1. Dout m (or n, o, p) = data-out from column m (or column n, column o, column p).
2. BL = 4 in the cases shown.
3. READs are to an active row in any bank.
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.

Truncated READs

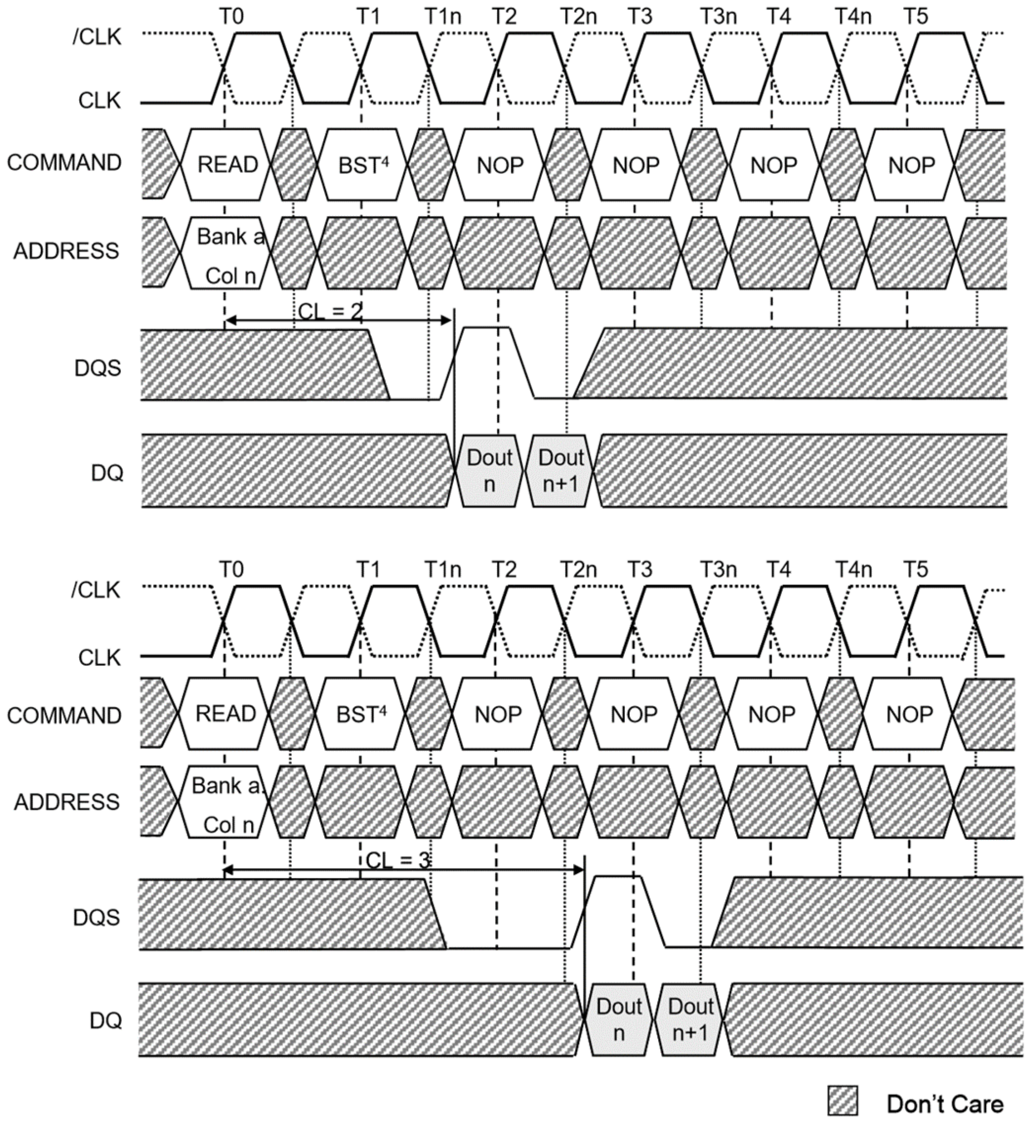
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 13. The BURST TERMINATE latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 14. The tDQSS (MIN) case is shown; the tDQSS (MAX) case has a longer bus idle time. (tDQSS [MIN] and tDQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the n- prefetch architecture). This is shown in Figure 15. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

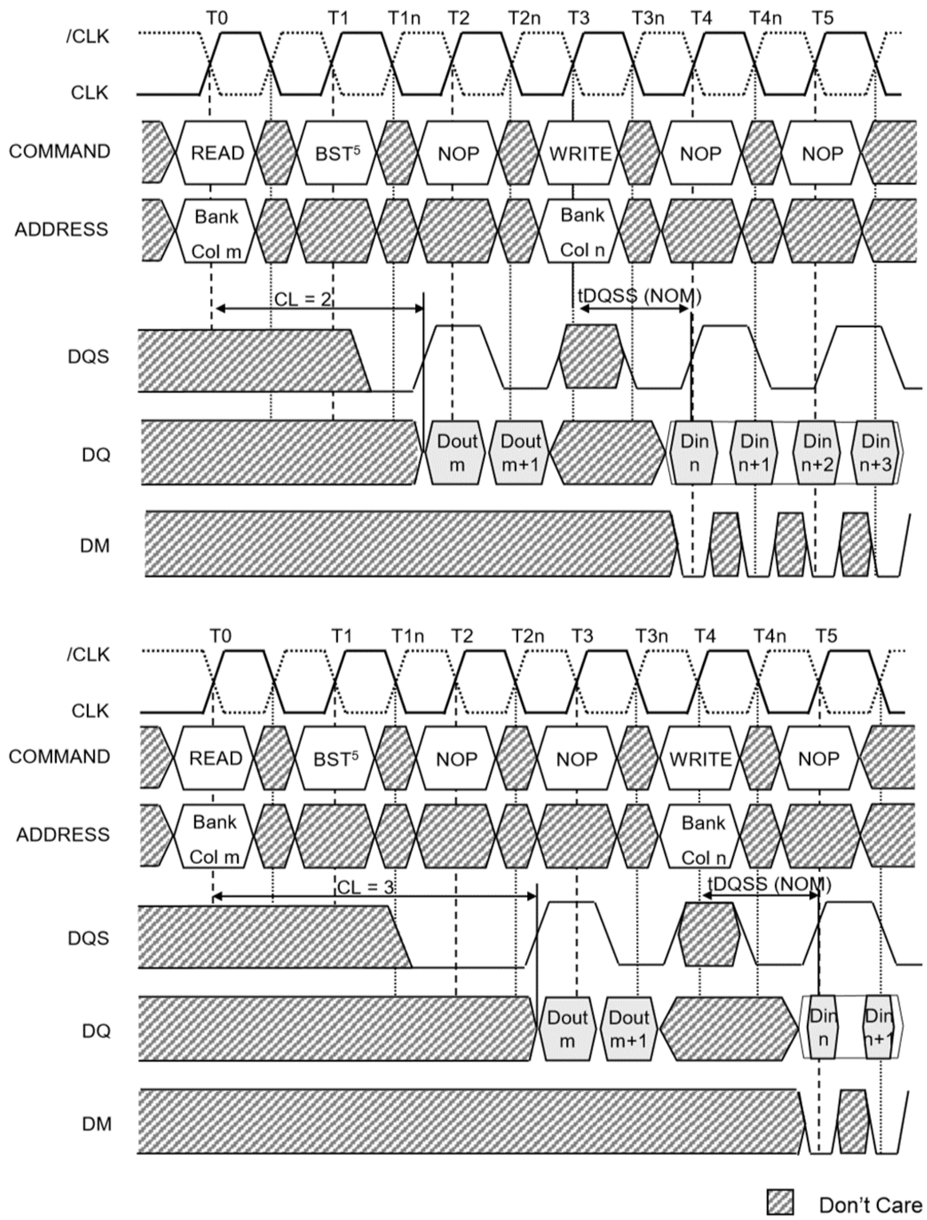
Note: Part of the row precharge time is hidden during the access of the last data elements.

Figure 13. READ Burst Terminated



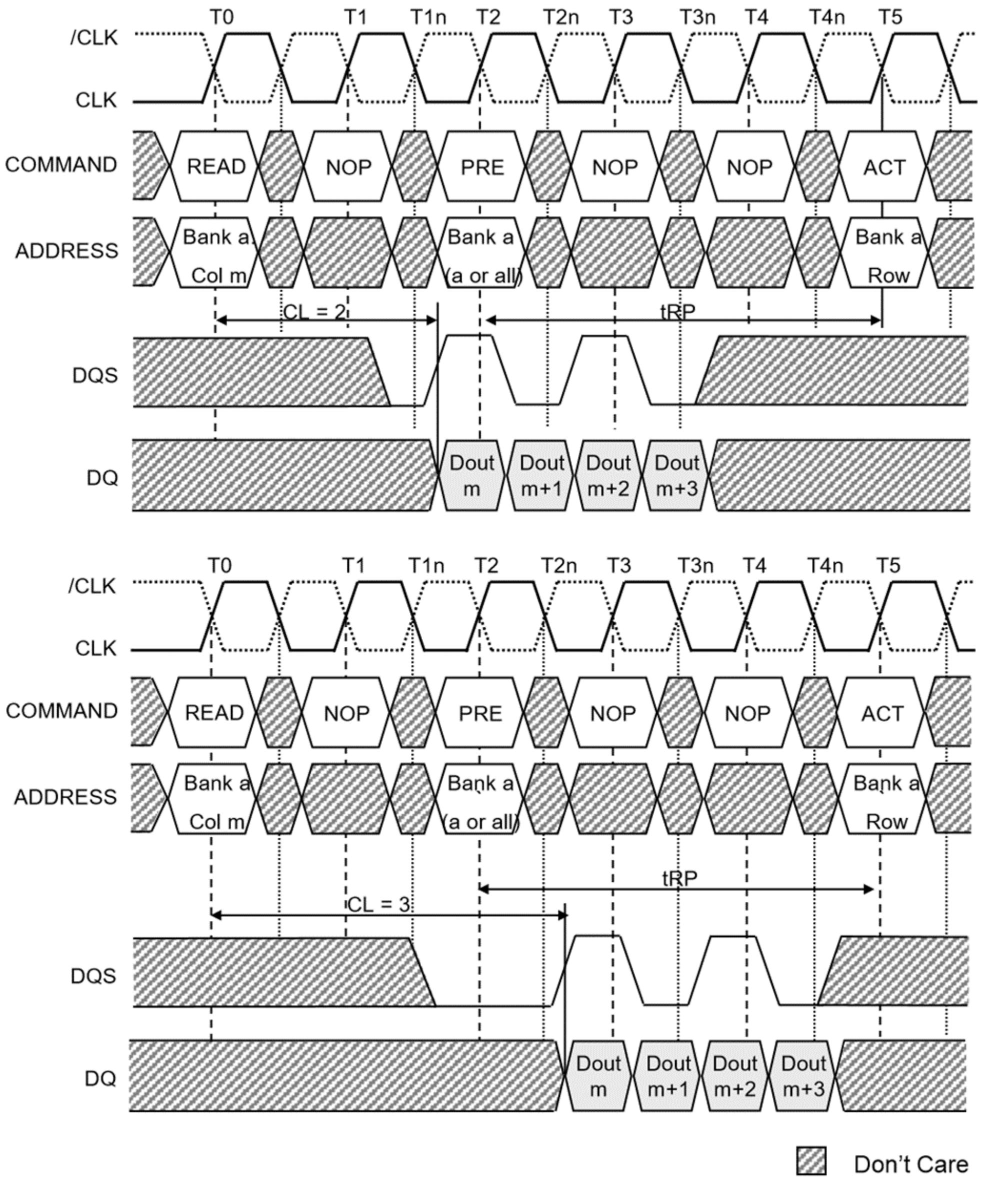
Notes:
1. Dout n = data-out from column n.
2. Only valid for BL = 4 and BL = 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. BST = BURST TERMINATE command; page remains open.
5. CKE = HIGH.

Figure 14. READ-to-WRITE Operation



Notes:
1. Dout m = data-out from column m.
2. Din n = data-in from column n.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal tAC, tDQSCLK, and tDQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.

Figure 15. READ-to-PRECHARGE Operation



Notes:

1. Dout m = data-out from column m.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal tAC, tDQSCLK, and tDQSQ.
4. READ-to-PRECHARGE equals 2 clocks, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided tRAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL / 2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.

WRITE

WRITE bursts are initiated with a WRITE command, as shown in Figure 16. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS [MIN] and tDQSS [MAX]) might not be intuitive, they have also been included. Figure 17 shows the nominal case and the extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

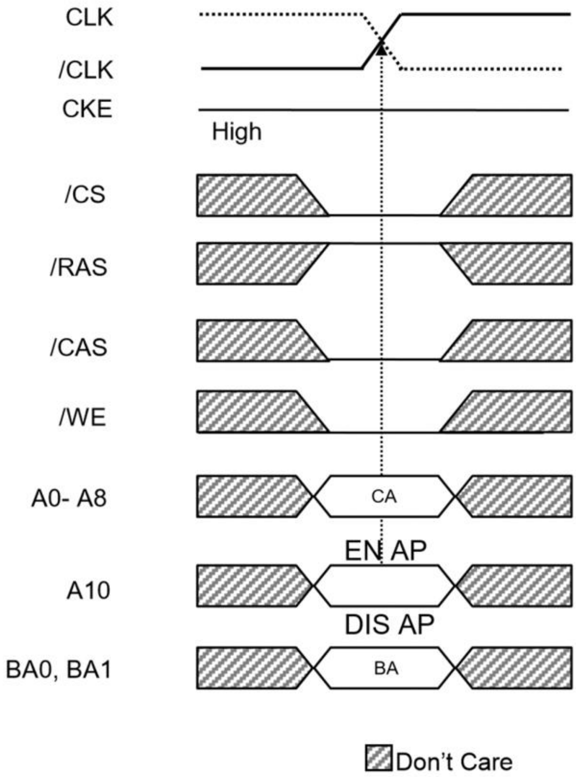
Figure 18 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 19. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 20. Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, tWTR should be met, as shown in Figure 21.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 22. Note that only the data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 23.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, tWR should be met, as shown in Figure 24.

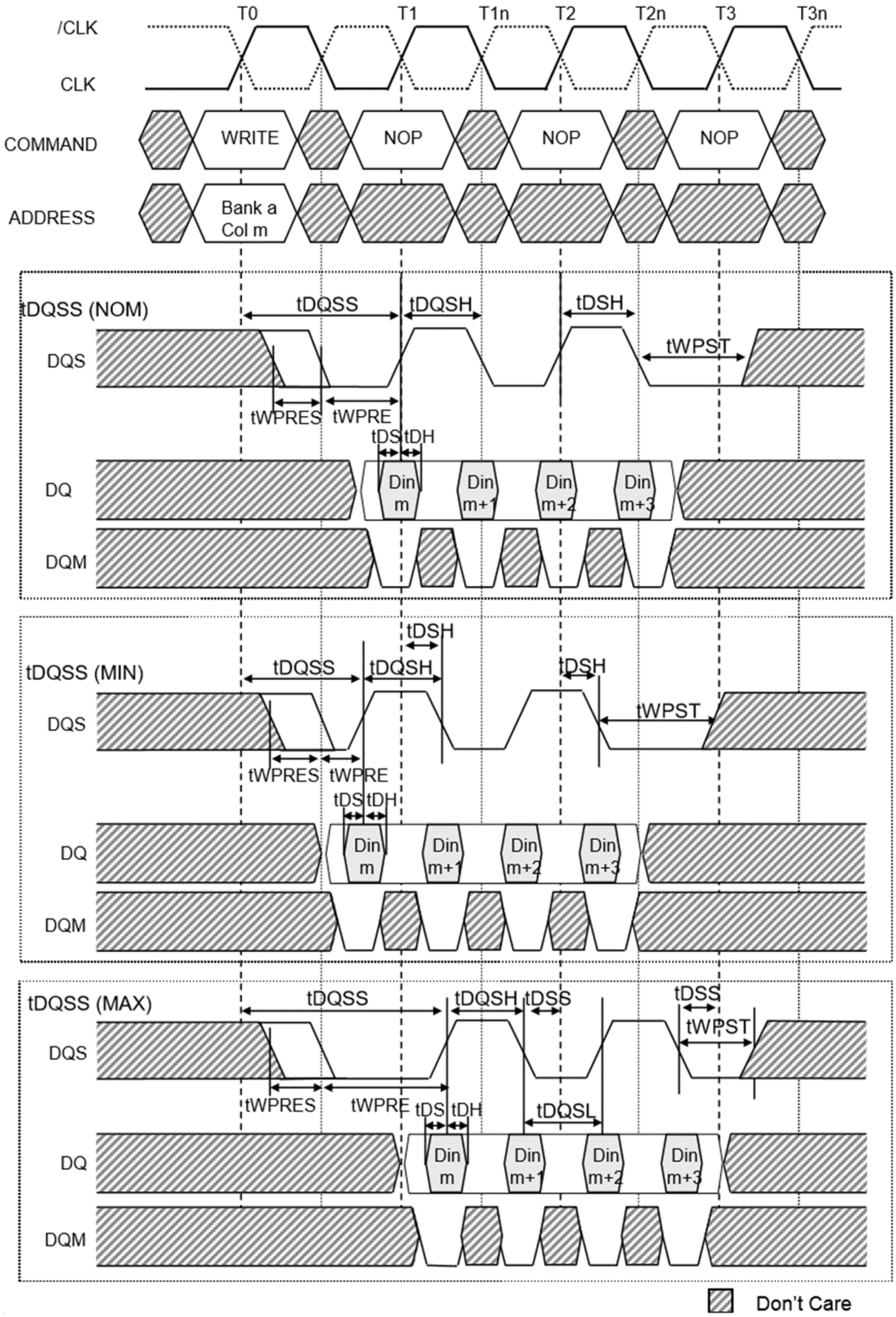
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 25 and Figure 26. Note that only the data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 25 and Figure 26. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

Figure 16. WRITE Command



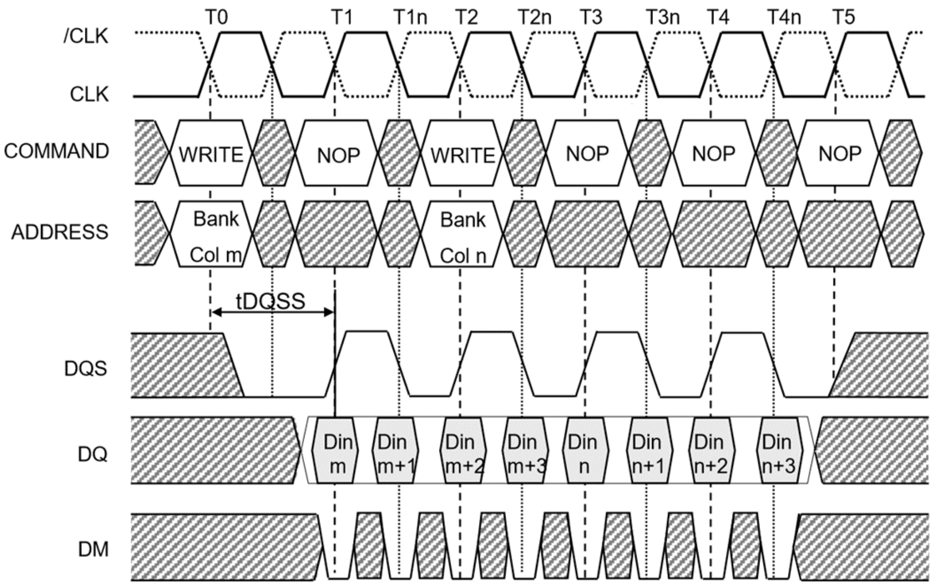
Notes:
1. DIS AP = Disable Auto Precharge
2. EN AP = Enable Auto Precharge
3. BA = Bank Address
4. CA = Column Address

Figure 17. WRITE Operation



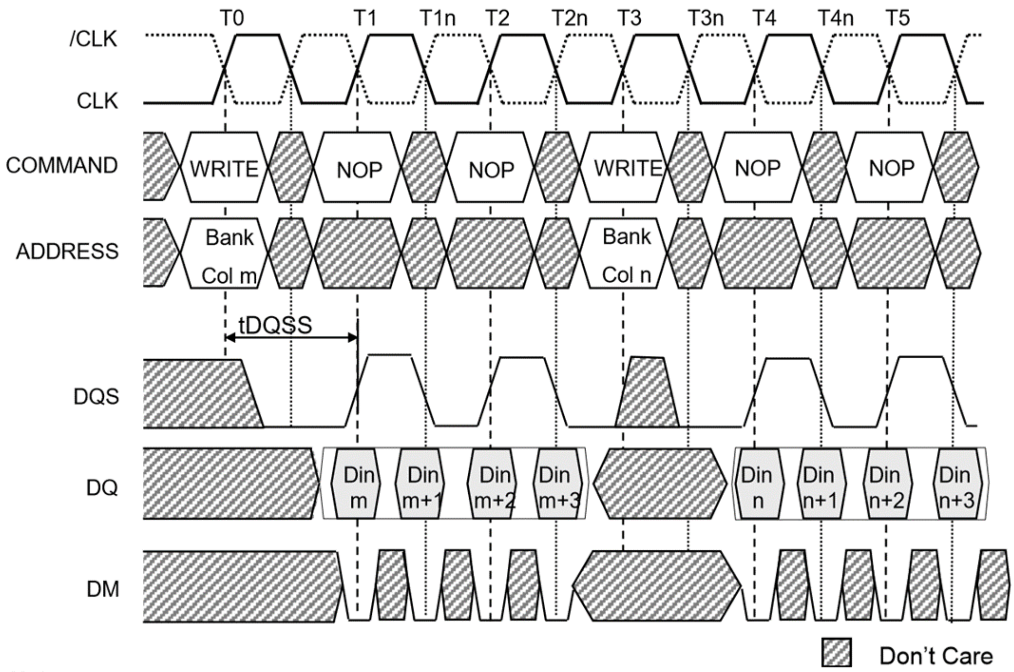
Notes:
1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 18. Consecutive WRITE-to-WRITE



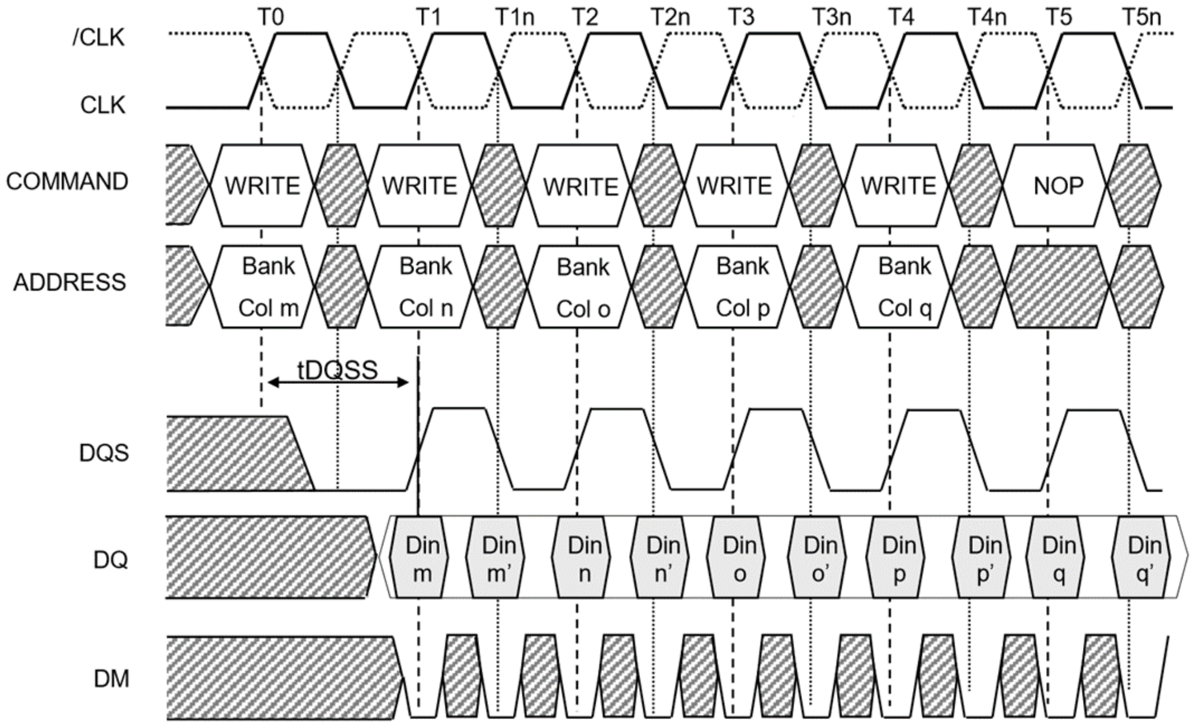
Notes:
1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

Figure 19. WRITE-to-WRITE Operation



Notes:
1. Din m (n) = data-in for column m (n).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

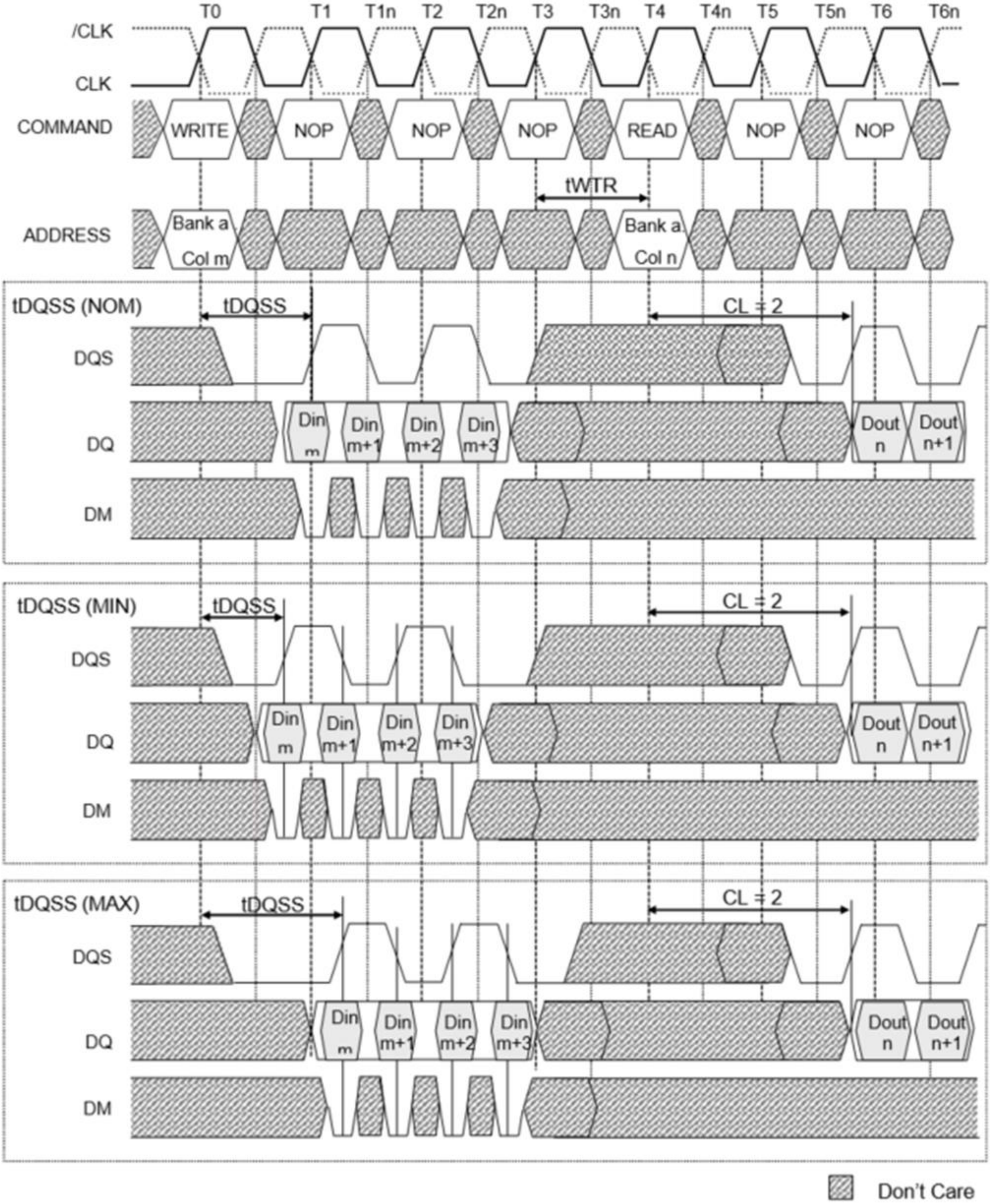
Figure 20. Random WRITE Cycles



Notes:

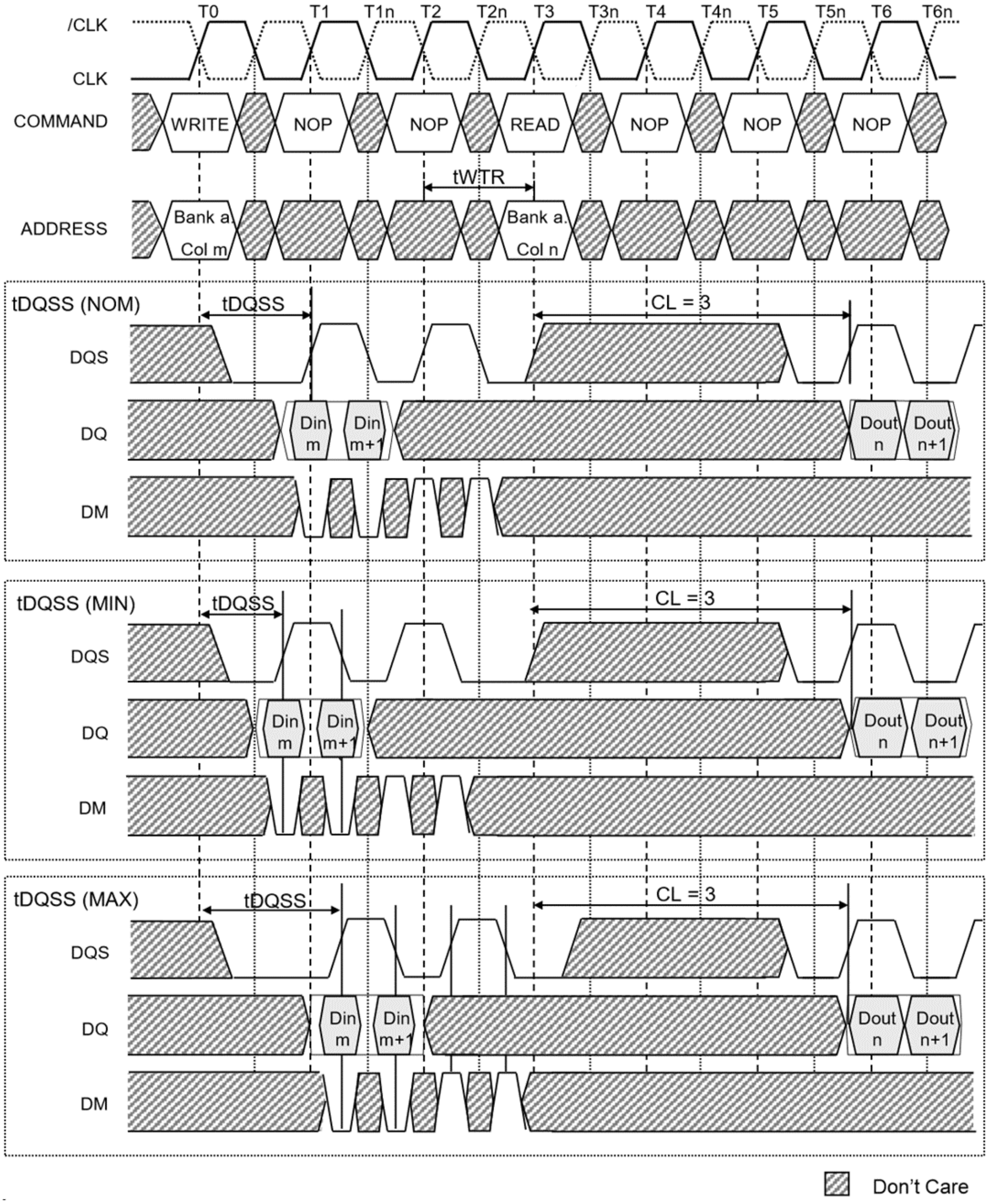
1. Din m (or n, o, p, q) = data-in for column m (or n, o, p, q)
2. m' (or n, o, p, q) = the next data-in following Din m (or n, o, p, q), according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.

Figure 21. WRITE-to-READ – Uninterrupting



Notes:
1. Din m = data-in for column m; Dout n = data-out for column n.
2. An uninterrupted burst of 4 is shown.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. The READ and WRITE commands are to same device. However, the READ and WRITE commands may be to different devices, in which case tWTR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

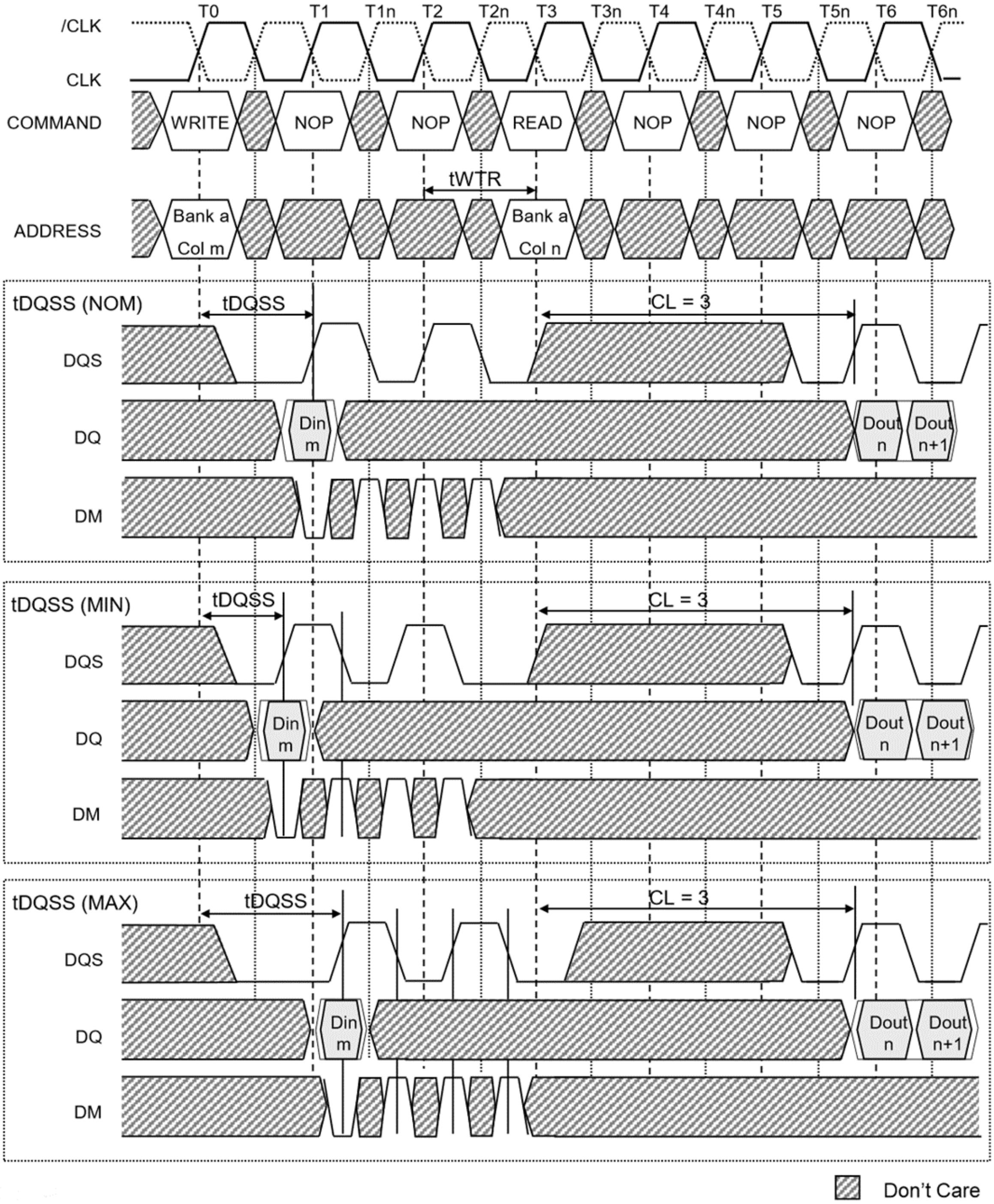
Figure 22. WRITE-to-READ – Interrupting



Notes:

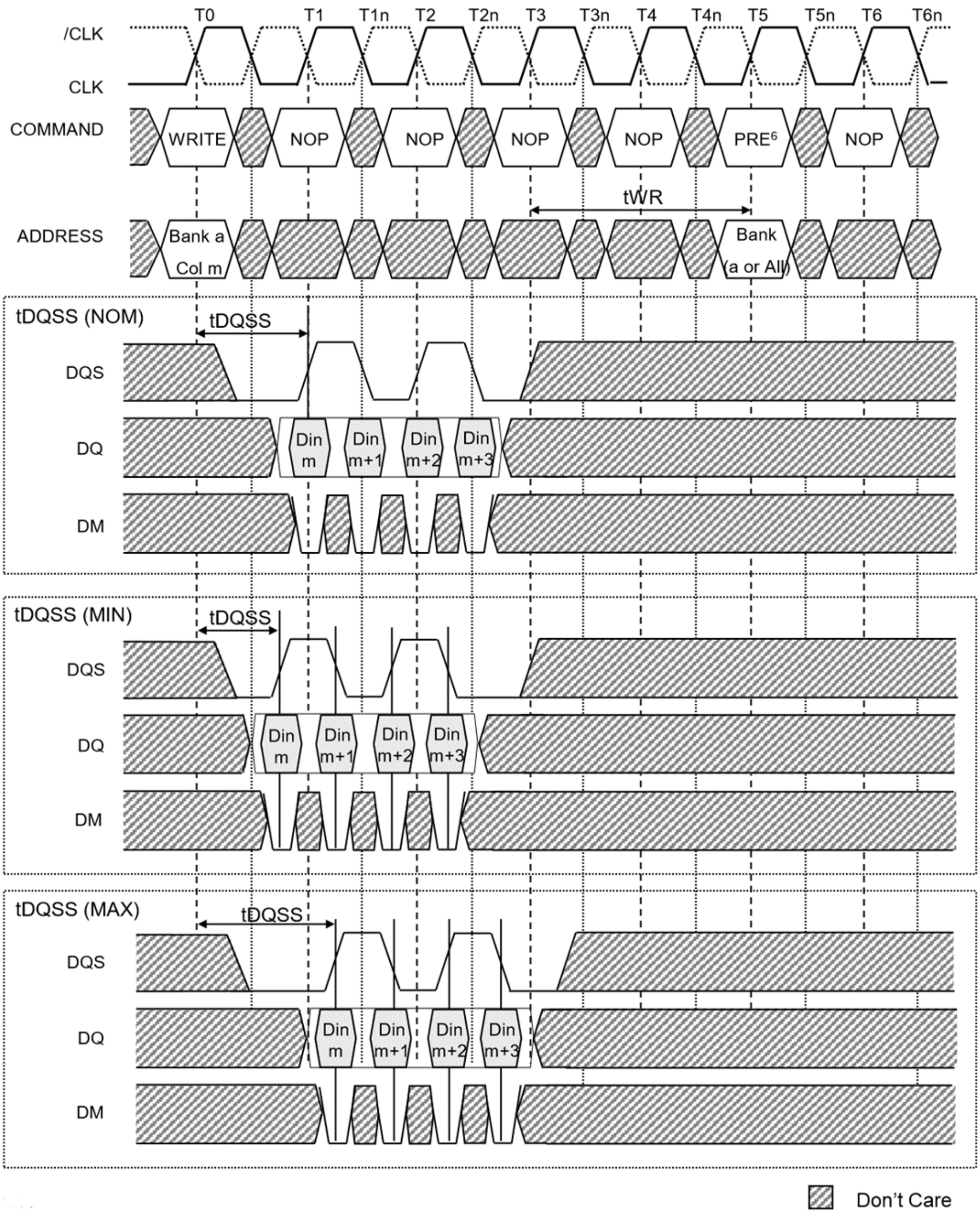
1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

Figure 23. WRITE-to-READ – Odd Number of Data, Interrupting



Notes:
1. Din m = data-in for column m; Dout n = data-out for column n.
2. An interrupted burst of 4 is shown; two data elements are written, three are masked.
3. tWTR is referenced from the first positive CLK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used and RD is required at T5, DM and DQS would be required at T4 and T4n because the READ command would not mask these two data elements.

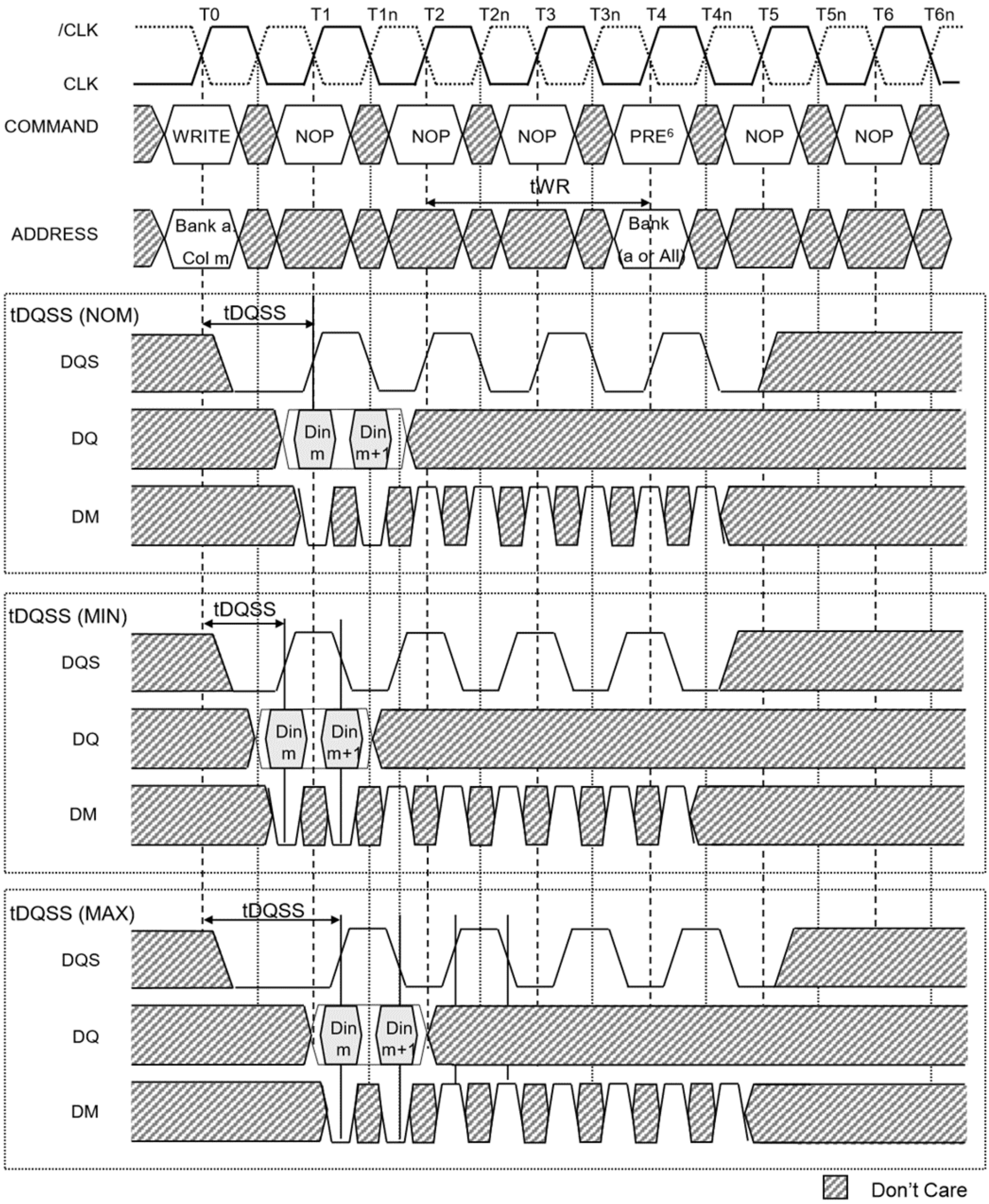
Figure 24. WRITE-to-PRECHARGE – Uninterrupting



Notes:

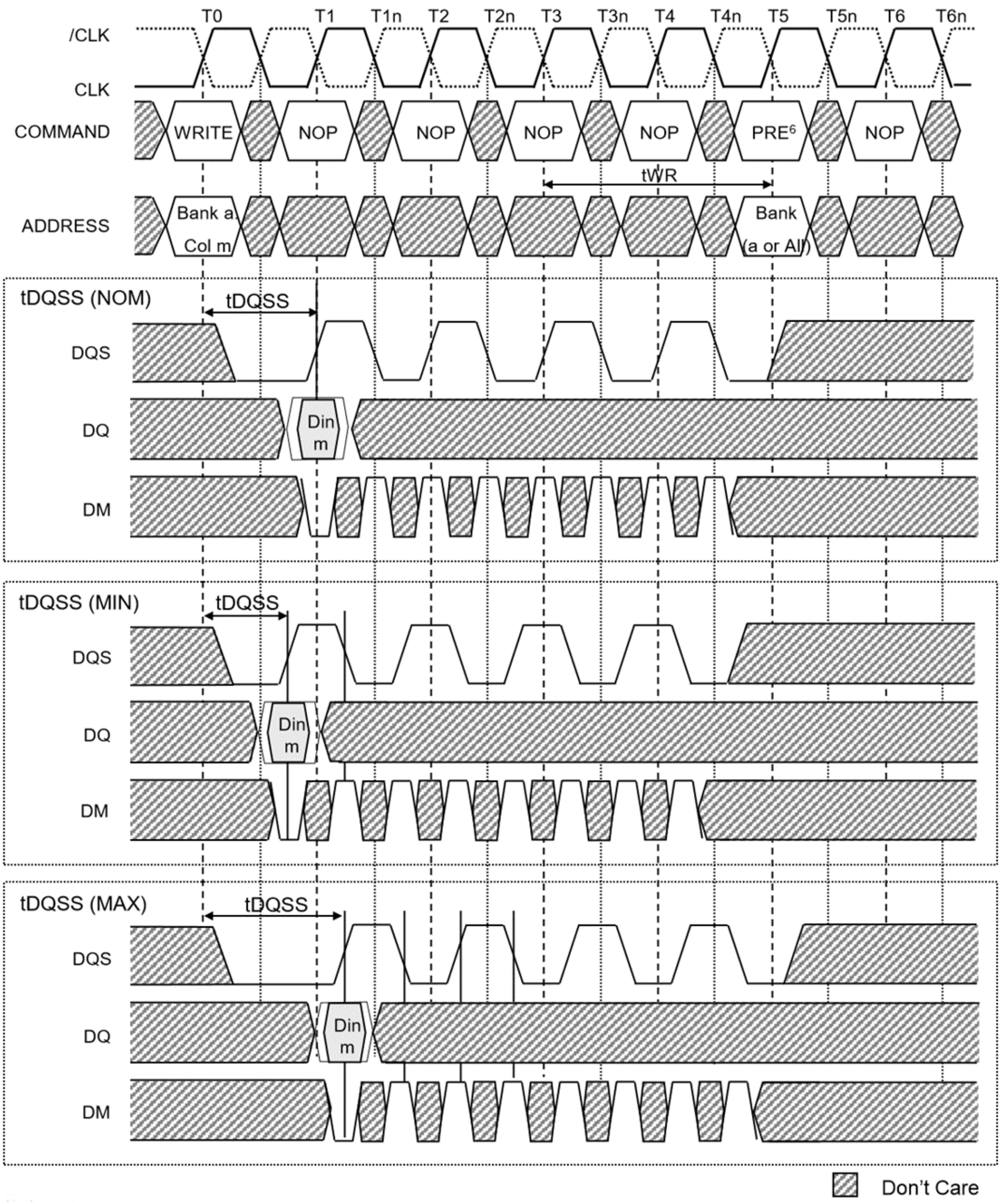
1. Din m = data-in for column m.
2. An uninterrupted burst of 4 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

Figure 25. WRITE-to-PRECHARGE – Interrupting



Notes:
1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

Figure 26. WRITE-to-PRECHARGE – Odd Number of Data, Interrupting



Notes:
1. Din m = data-in for column m.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CLK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case tWR is not required and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.

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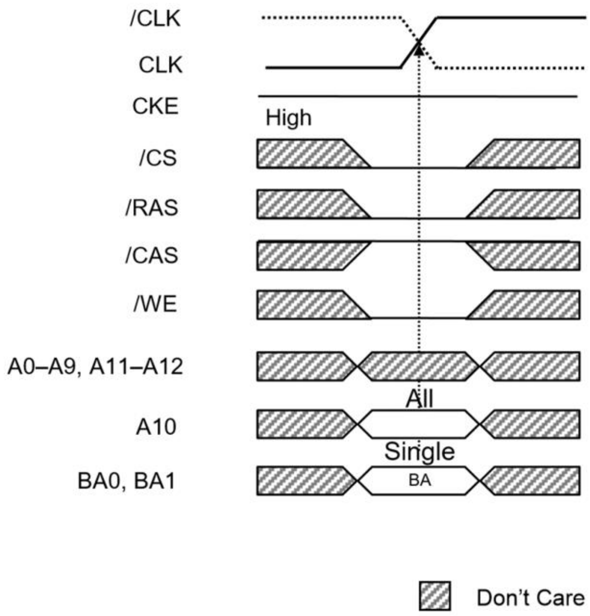
PRECHARGE

The PRECHARGE command (Figure 27) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 27. PRECHARGE Command



Notes:
1. BA = Bank Address.
2. All = All banks to be Precharged, BA1, BA0 are “Don't Care.”
3. Single = Only bank selected by BA1 and BA0 will be precharged

Power-Down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst; thus a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.

Power-Down (Active or Precharge)

Power-down (Figure 28) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, including CLK and /CLK. Exiting power-down requires the device to be at the same voltage as when it entered power-down and a stable clock.

Note:

The power-down duration is limited by the refresh requirements of the device. While in power-down, CKE LOW must be maintained at the inputs of the Low Power DDR SDRAM, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until tPDX is satisfied.

Figure 28. Power-Down Command (Active or Precharge)

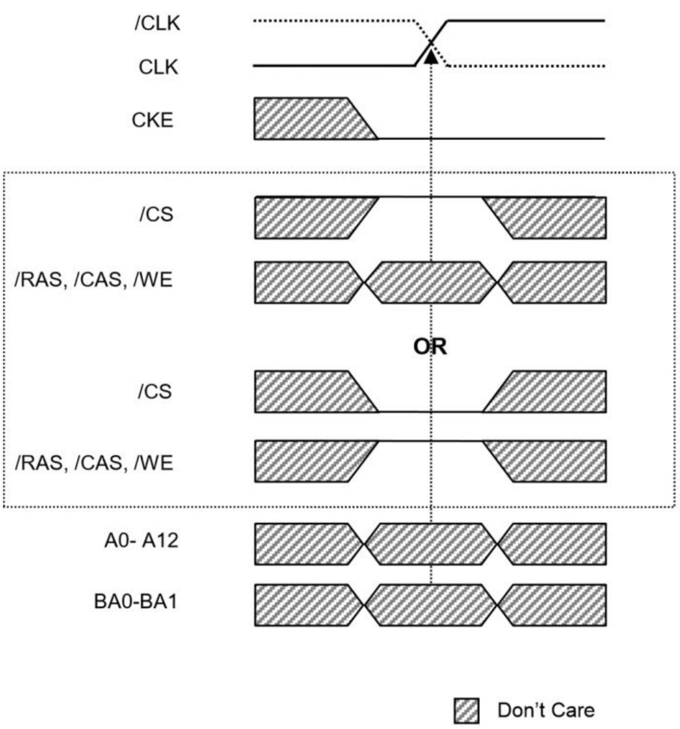


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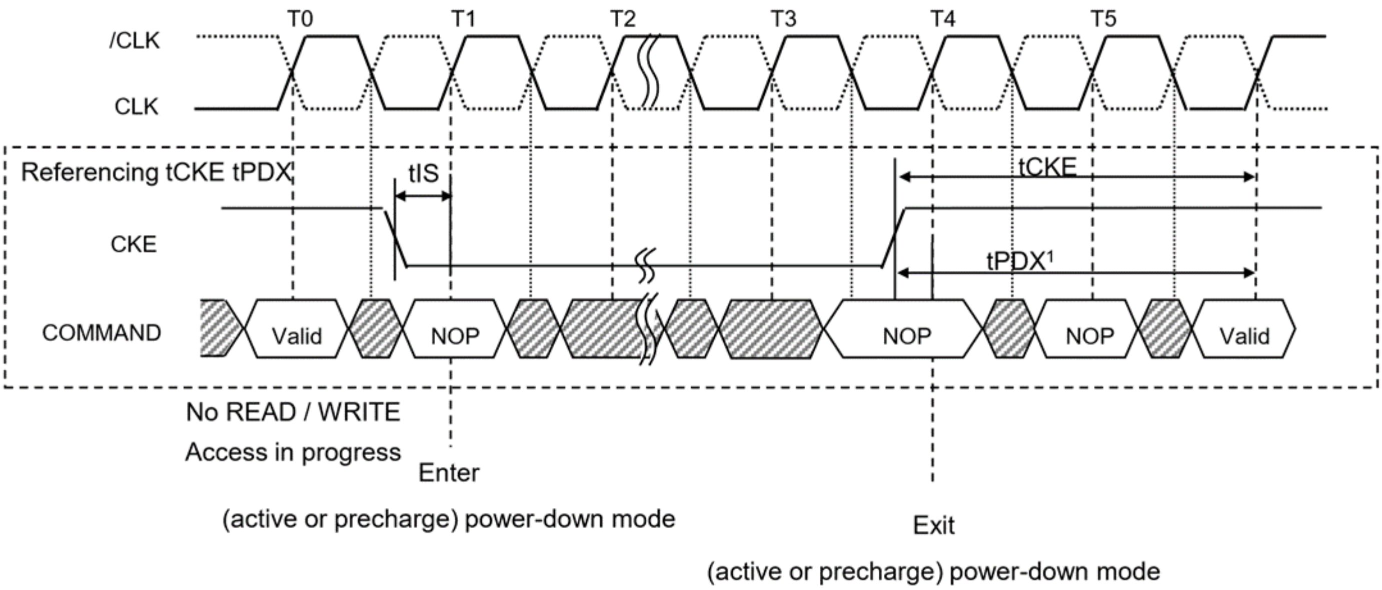
Figure 29. Power-Down (Active or Precharge)



Note: Clock must toggle a minimum of once during this time

Truth Tables

Table 16. Truth Table – CKE

Notes: 1–5

CKEn-1	CKEn	Current State	COMMANDn	ACTIONn	Notes
L	L	(Active) Power-Down	X	Maintain (active) power-down	
L	L	(Precharge) Power-Down	X	Maintain (precharge) power-down	
L	L	Self refresh	X	Maintain self refresh	
L	H	(Active) Power-Down	DESELECT or NOP	Exit (active) power-down	6, 7
L	H	(Precharge) Power-Down	DESELECT or NOP	Exit (precharge) power-down	6, 7
L	H	Self refresh	DESELECT or NOP	Exit self refresh	8, 9
H	L	Bank(s) active	DESELECT or NOP	(Active) power-down entry	
H	L	All banks idle	DESELECT or NOP	(Precharge) power-down entry	
H	L	All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 18		
H	H		See Table 18		

Notes:
1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. tCKE pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the tPDX period.
7. The clock must toggle at least once during the tPDX period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSR period.
9. The clock must toggle at least once during the tXSR period.

Table 17. Truth Table – Current State Bank n - Command to Bank n

Notes: 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes:

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) and after tPDX has been met (if the previous state was power-down).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated. Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 16, and according to Table17.

   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the row active state.

   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the DDR SDRAM will be in the all banks idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. Once tMRD is met, the Low Power DDR SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 18. Truth Table – Current State Bank n - Command to Bank m

Notes: 1–6; notes appear below and on next page

Current State	/CS	/RAS	/CAS	/WE	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7. 9, 3a
	L	L	H	L	PRECHARGE	
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes:

1. This table applies when CKE*n*-1 was HIGH and CKEn is HIGH and after tXSR has been met (if the previous state was self refresh) or after tPDX has been met (if the previous state was power-down).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read with auto precharge enabled: See following text – 3a

   Write with auto precharge enabled: See following text – 3a

   3a. The read with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins.

   This device supports concurrent auto precharge such that when a read with auto precharge enabled or a write with auto precharge is enabled any command to other banks is allowed, long as that command does not interrupt the read or write data transfer already in process. either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

   3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

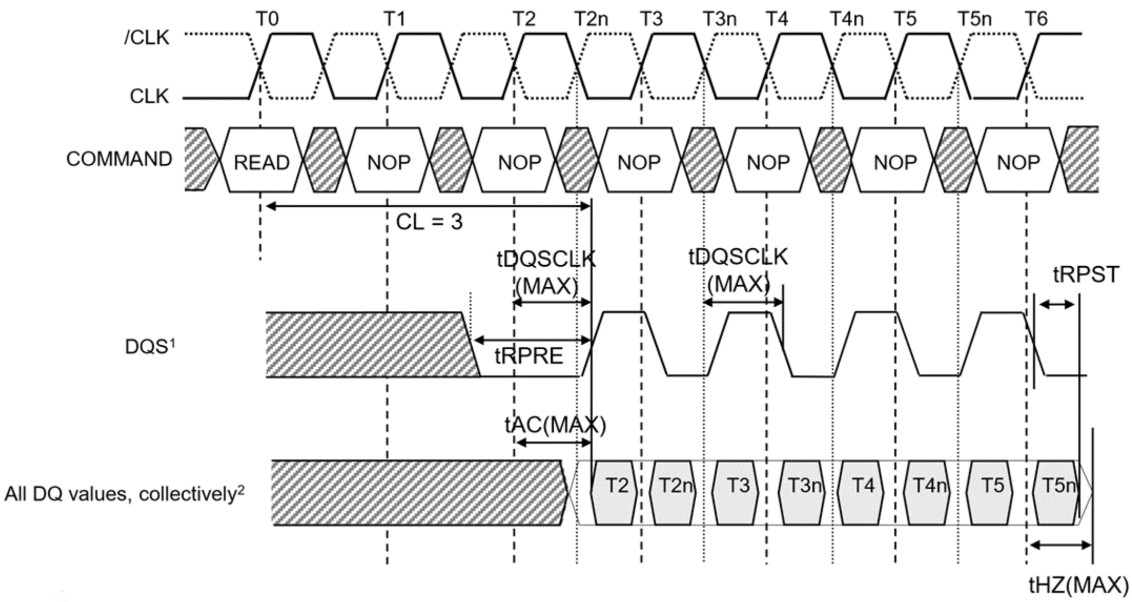
From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	[1 + (BL/2)] tCLK + tWTR
	WRITE or WRITE w/AP	(BL/2) tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK
READ w/AP	READ or READ w/AP	(BL/2) × tCLK
	WRITE or WRITE w/AP	[CLRU + (BL/2)] tCLK
	PRECHARGE	1 tCLK
	ACTIVE	1 tCLK

CLRU = CAS Latency (CL) rounded up to the next integer

BL = Burst Length

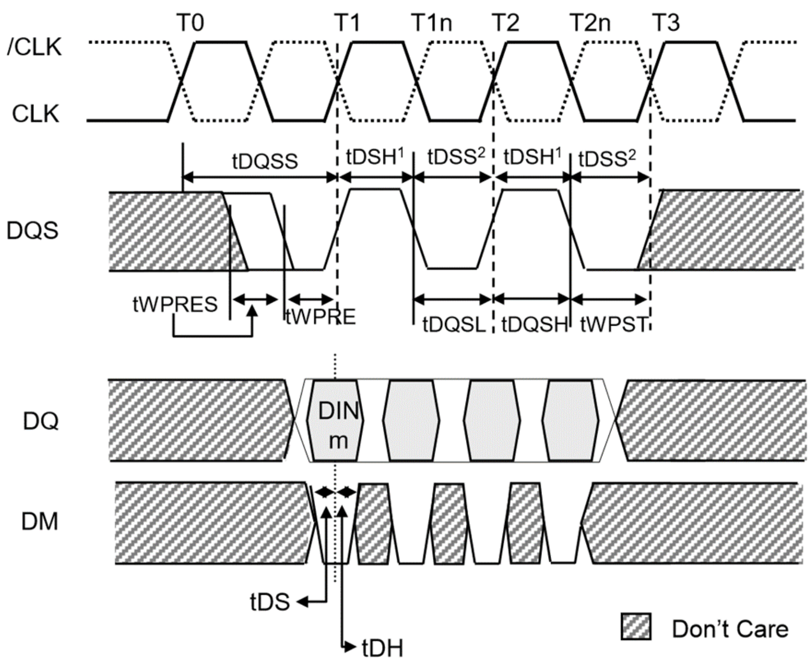
4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Figure 30. Data Output Timing – tAC and tDQSCLK



Notes:
1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CLK, and is the "long term" component of DQ skew.

Figure 31. Data Input Timing



Notes:
1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).
3. WRITE command issued at T0.

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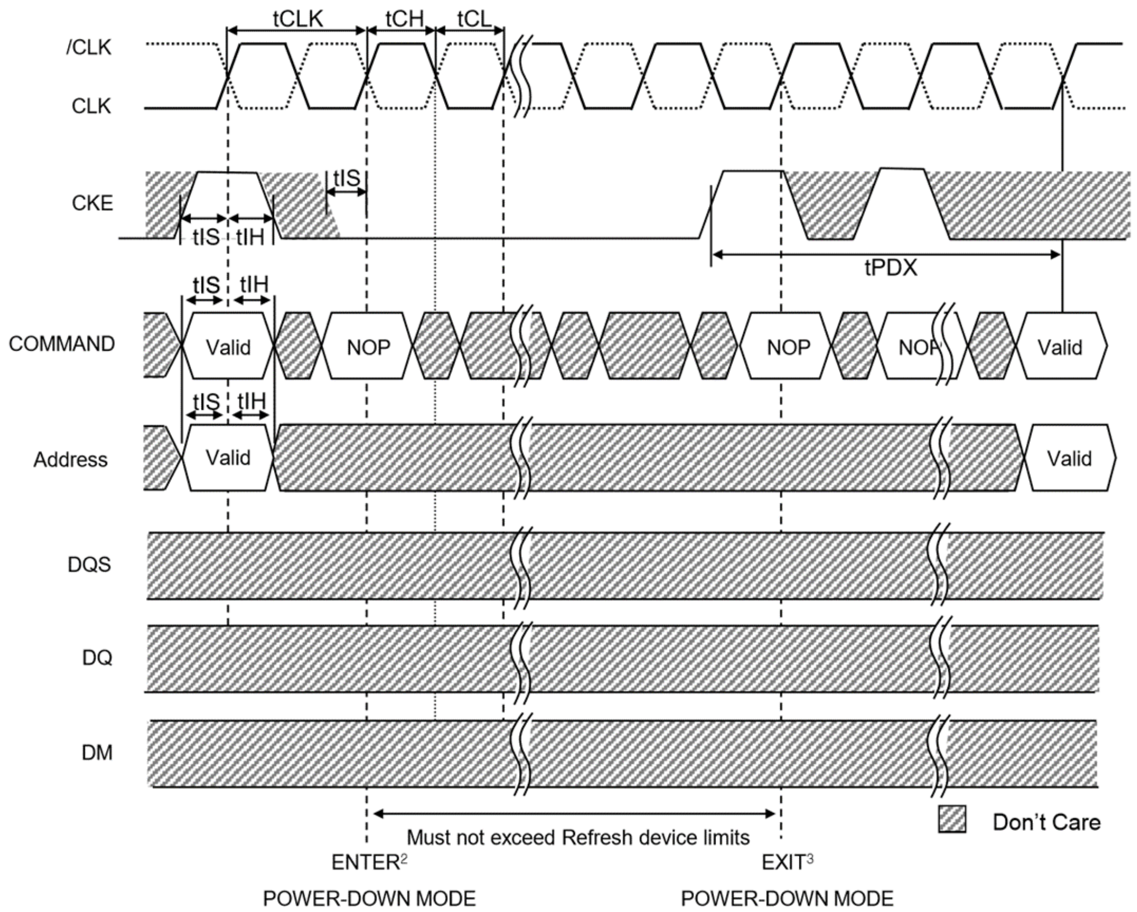
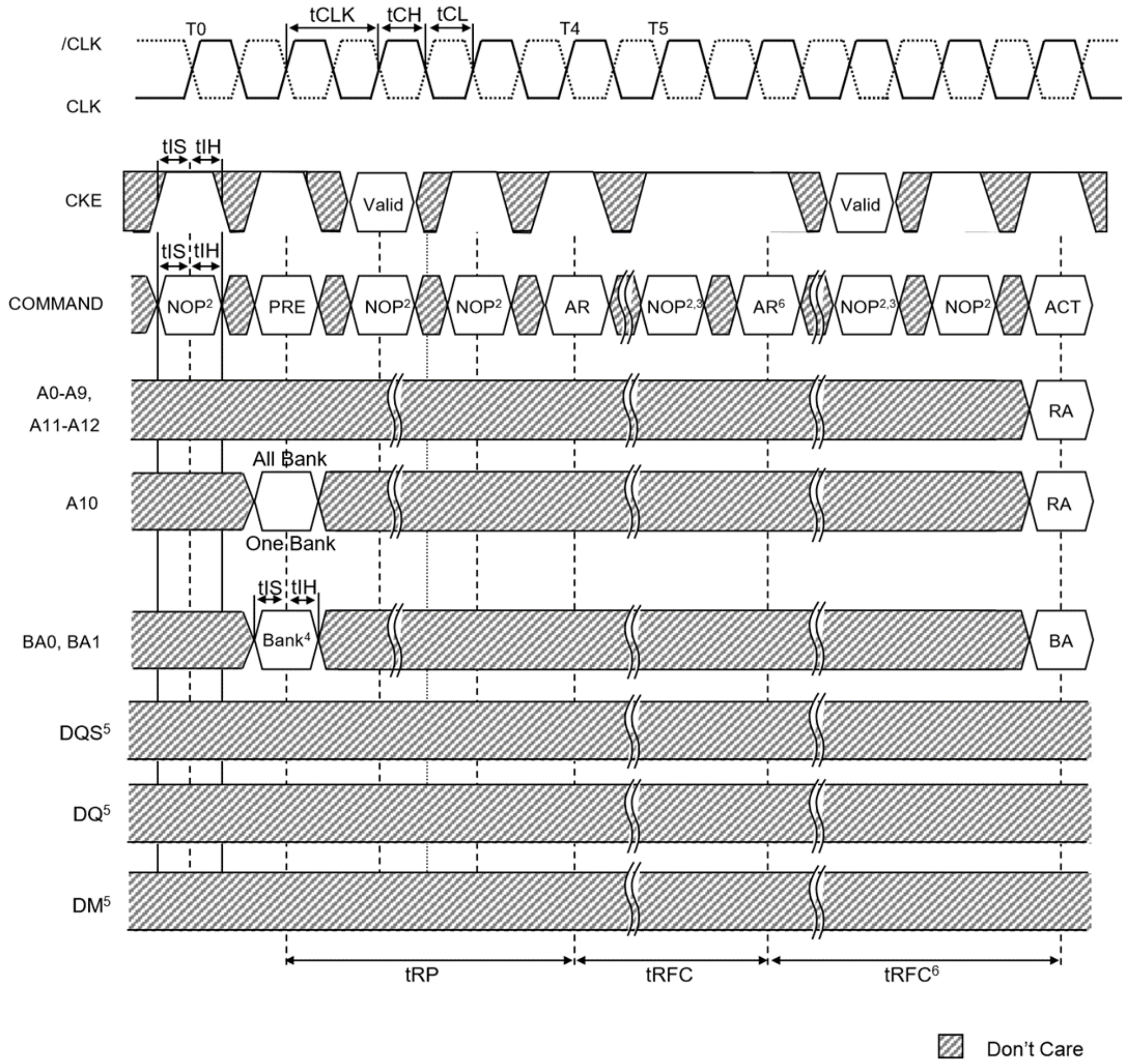
Figure 32. Power-Down Mode (Active or Precharge)



Notes:

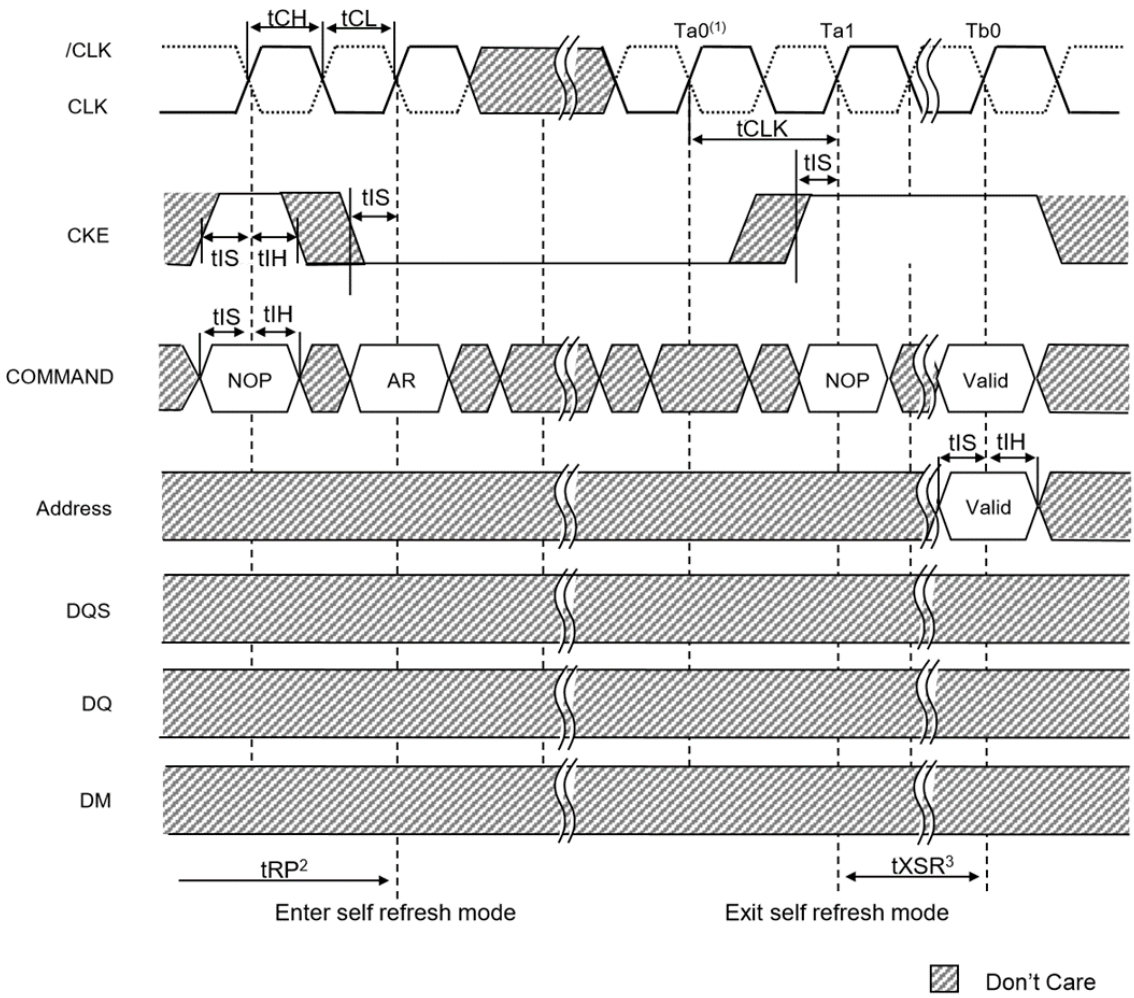
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during tPDX time.

Figure 33. Auto Refresh Mode



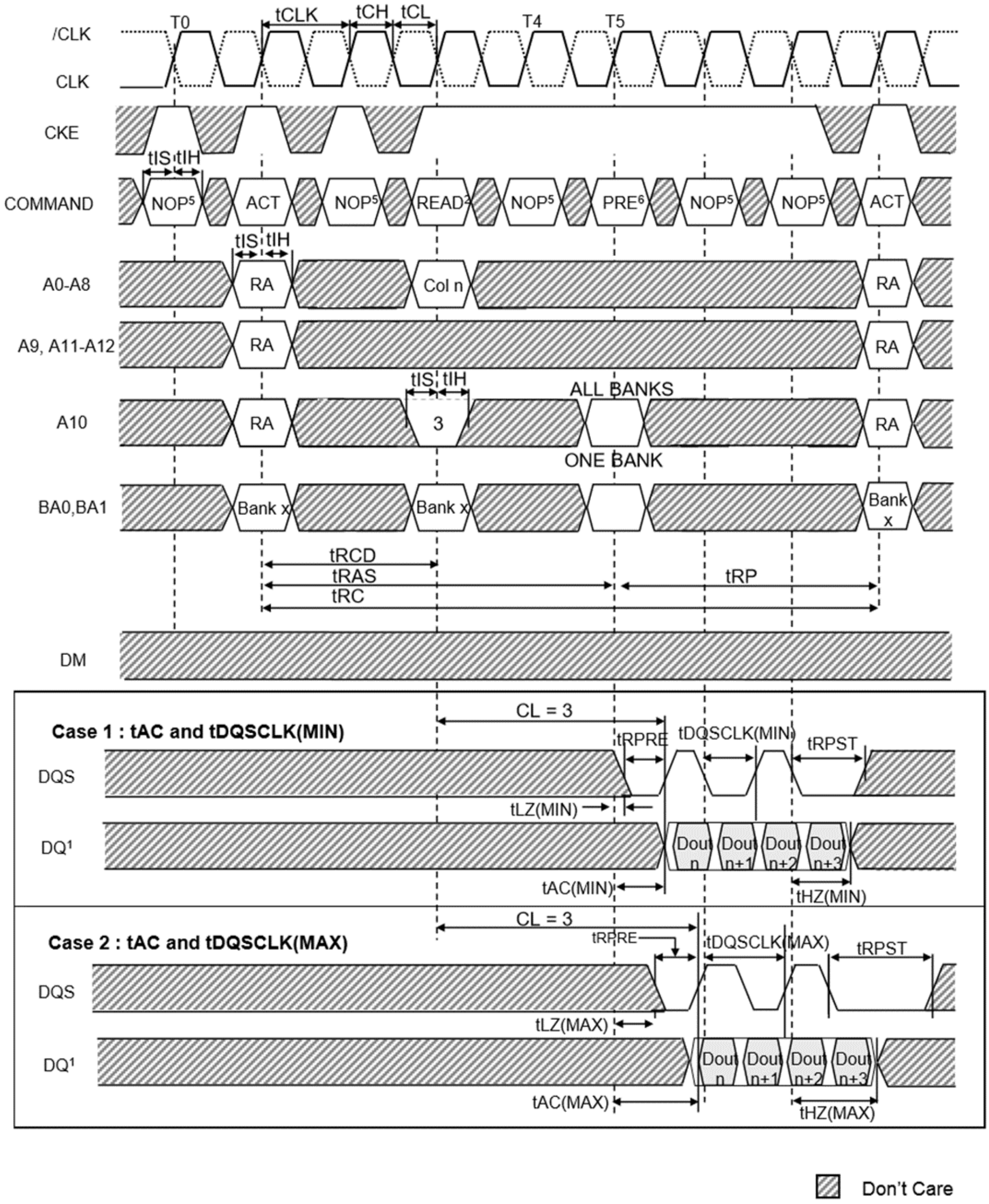
Notes:
1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row address, BA = Bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after tRFC time, CKE must be active during clock positive transitions.
4. “Don’t Care” if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
5. DM, DQ, and DQS signals are all “Don’t Care”/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

Figure 34. Self Refresh Mode



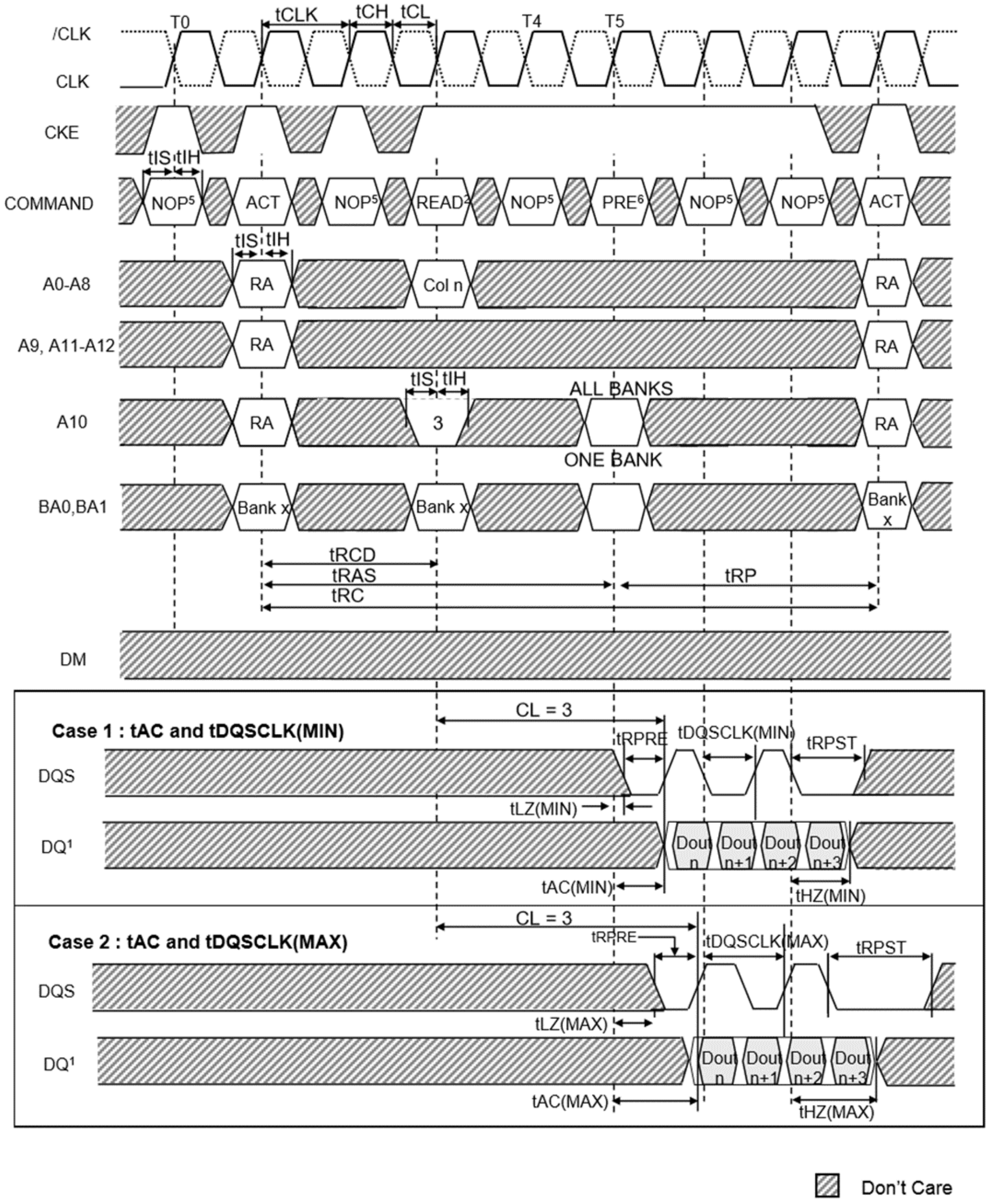
Notes:
1. Clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by Ta0.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT are required for tXSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.

Figure 35. Bank Read – Without Auto Precharge



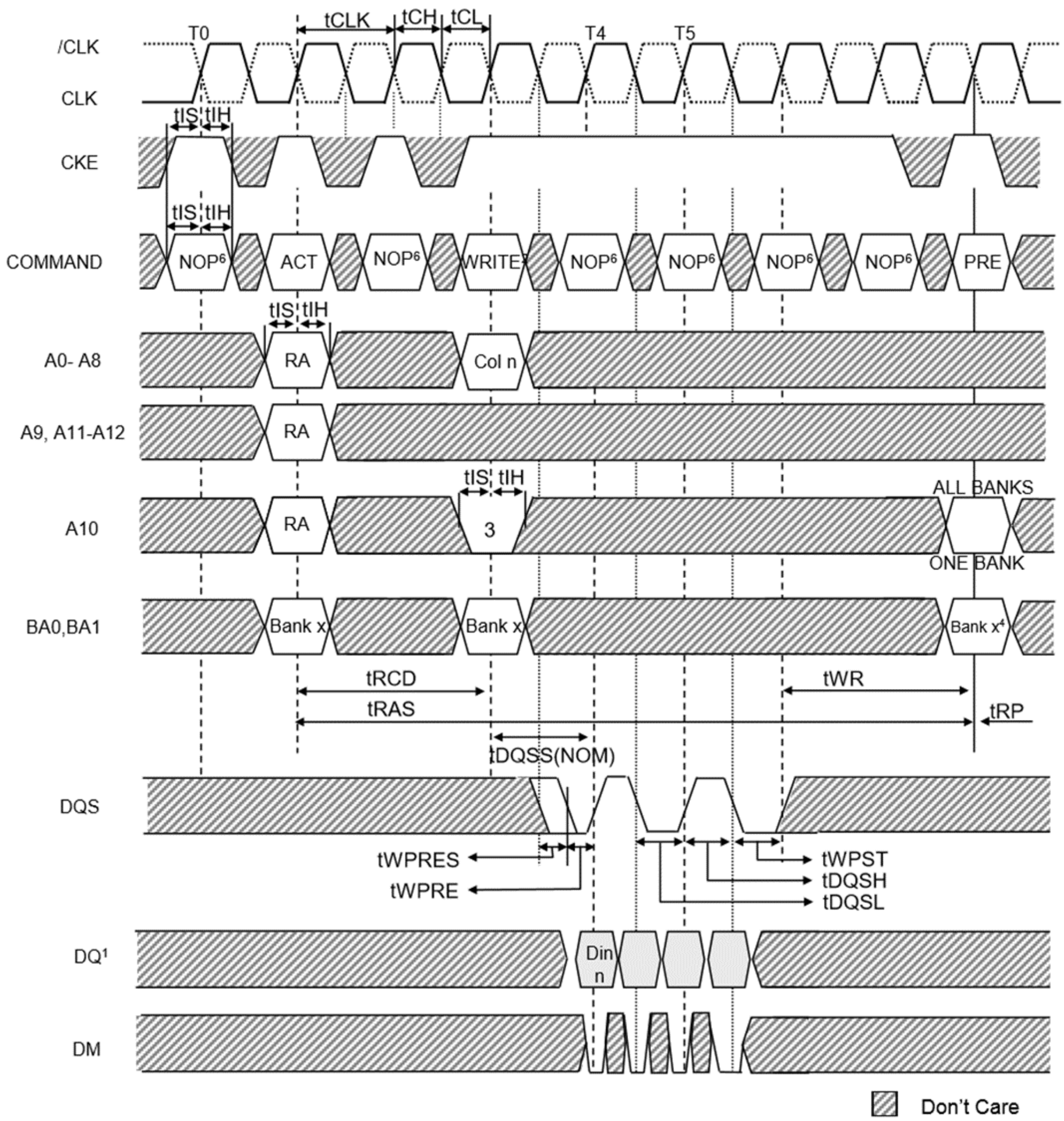
Notes:
1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The PRECHARGE command can only be applied at T5 if tRAS minimum is met.

Figure 36. Bank Read – With Auto Precharge



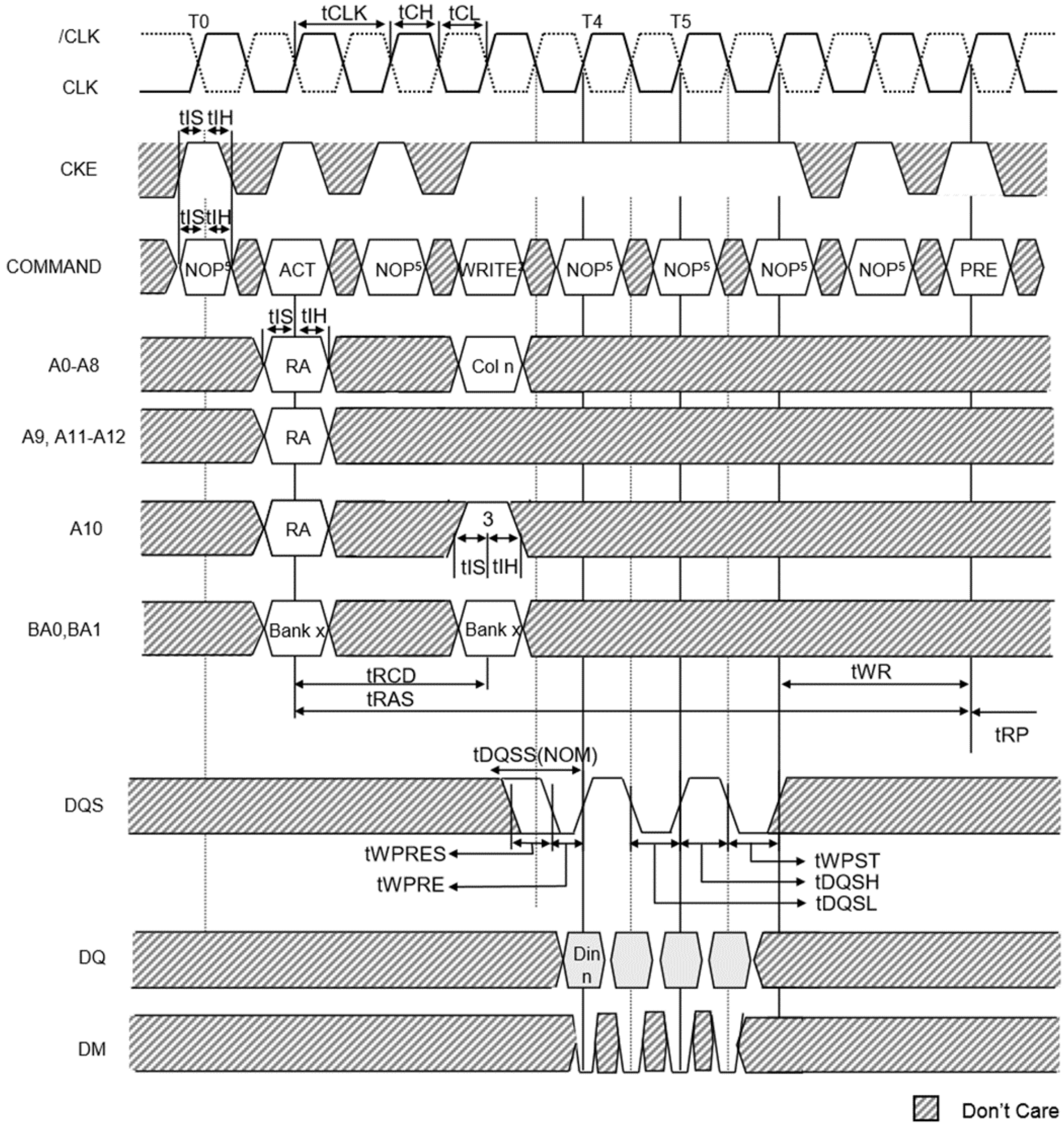
Notes:
1. Dout n = data-out from column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.

Figure 37. Bank Write – Without Auto Precharge



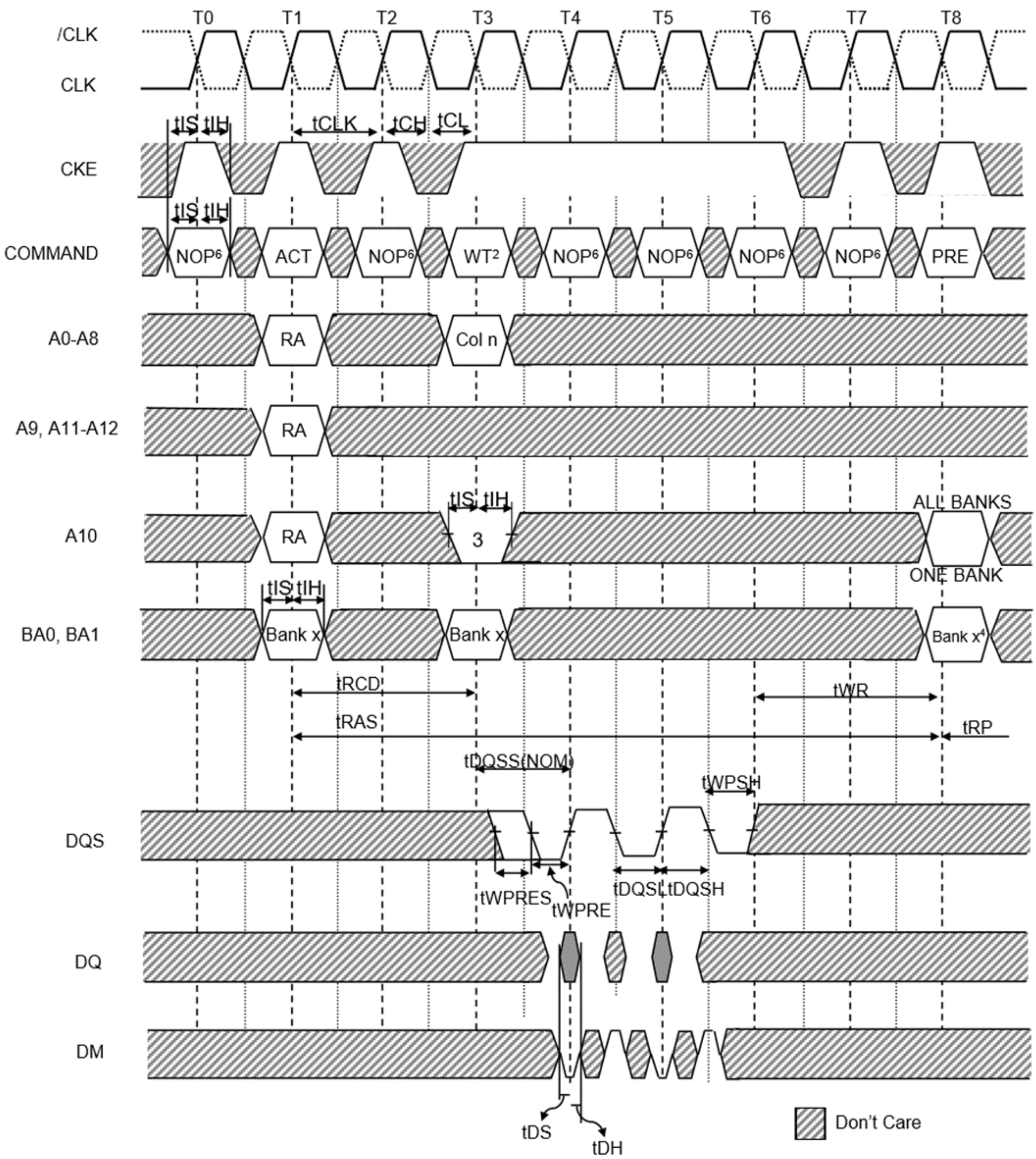
Notes:
1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. “Don’t Care” if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

Figure 38. Bank Write – With Auto Precharge



Notes:
1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
7. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

Figure 39. Write – DM Operation



Notes:
1. Din n = data-in for column n.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row address, BA = Bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. tDSH is applicable during tDQSS (MIN) and is referenced from tCLK T4 or T5.
8. tDSH is applicable during tDQSS (MAX) and is referenced from tCLK T5 or T6.

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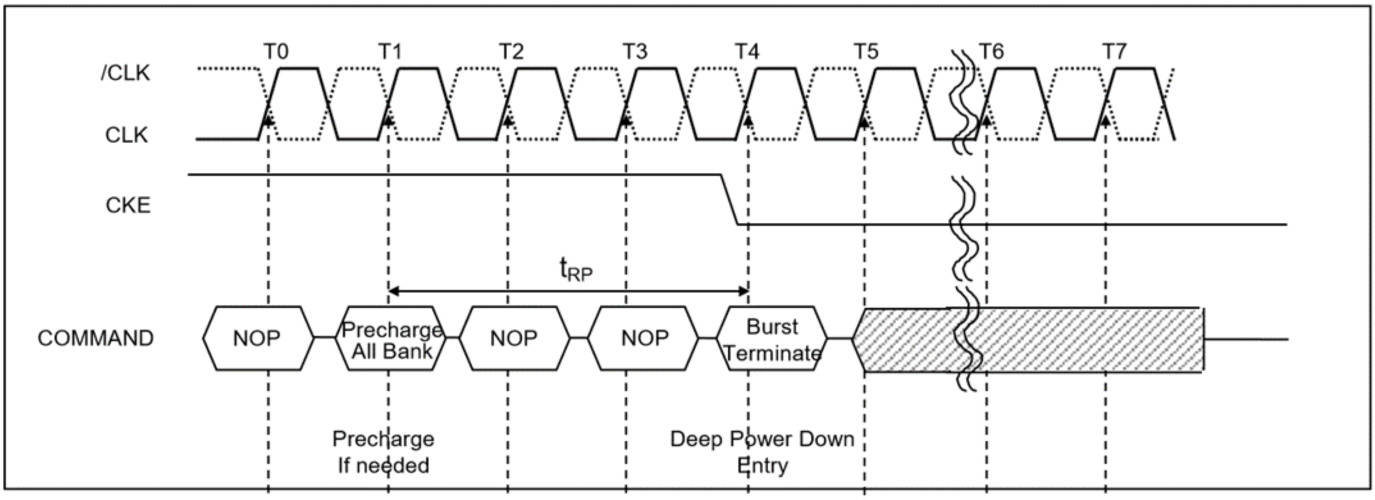
DEEP POWER DOWN MODE ENTRY

The Deep Power Down Mode is entered by having burst termination command, while CKE is low. The Deep Power Down Mode has to be maintained for a minimum of 100us. The following diagram illustrates Deep Power Down mode entry.

Figure 40. Deep Power Down Mode Entry



DEEP POWER DOWN MODE EXIT SEQUENCE

The Deep Power Down Mode is exited by asserting CKE high.
After the exit, the following sequence is needed to enter a new command

1. Maintain NOP input conditions for a minimum of 200us
2. Issue precharge commands for all banks of the device
3. Issue 2 or more auto refresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extended mode register

The following timing diagram illustrates deep power down exit sequence.

Figure 41. Deep Power Down Mode Exit

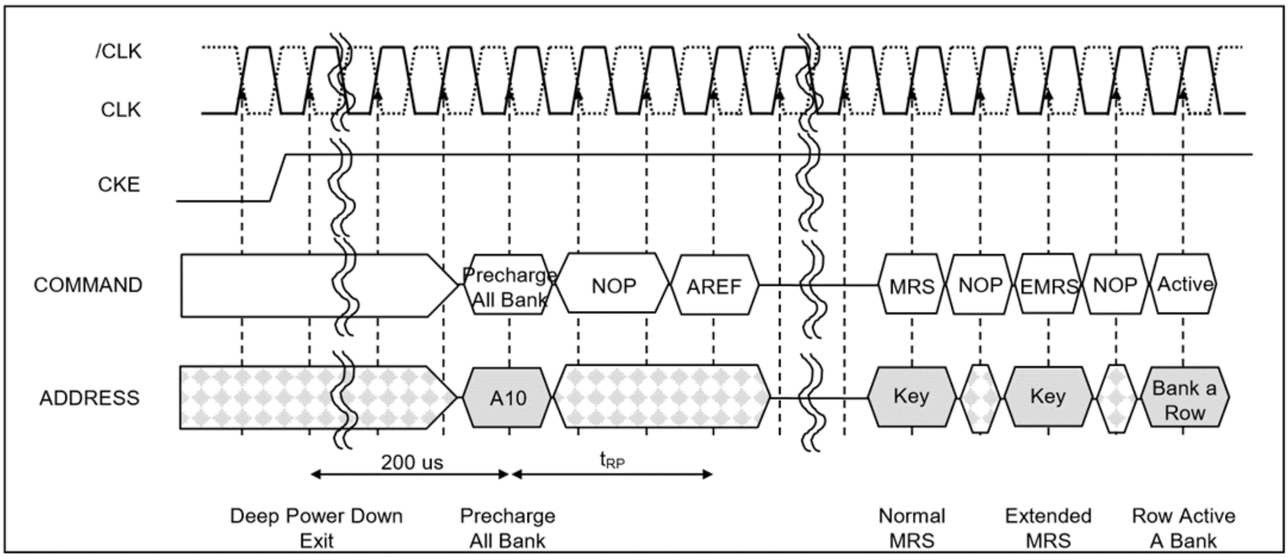


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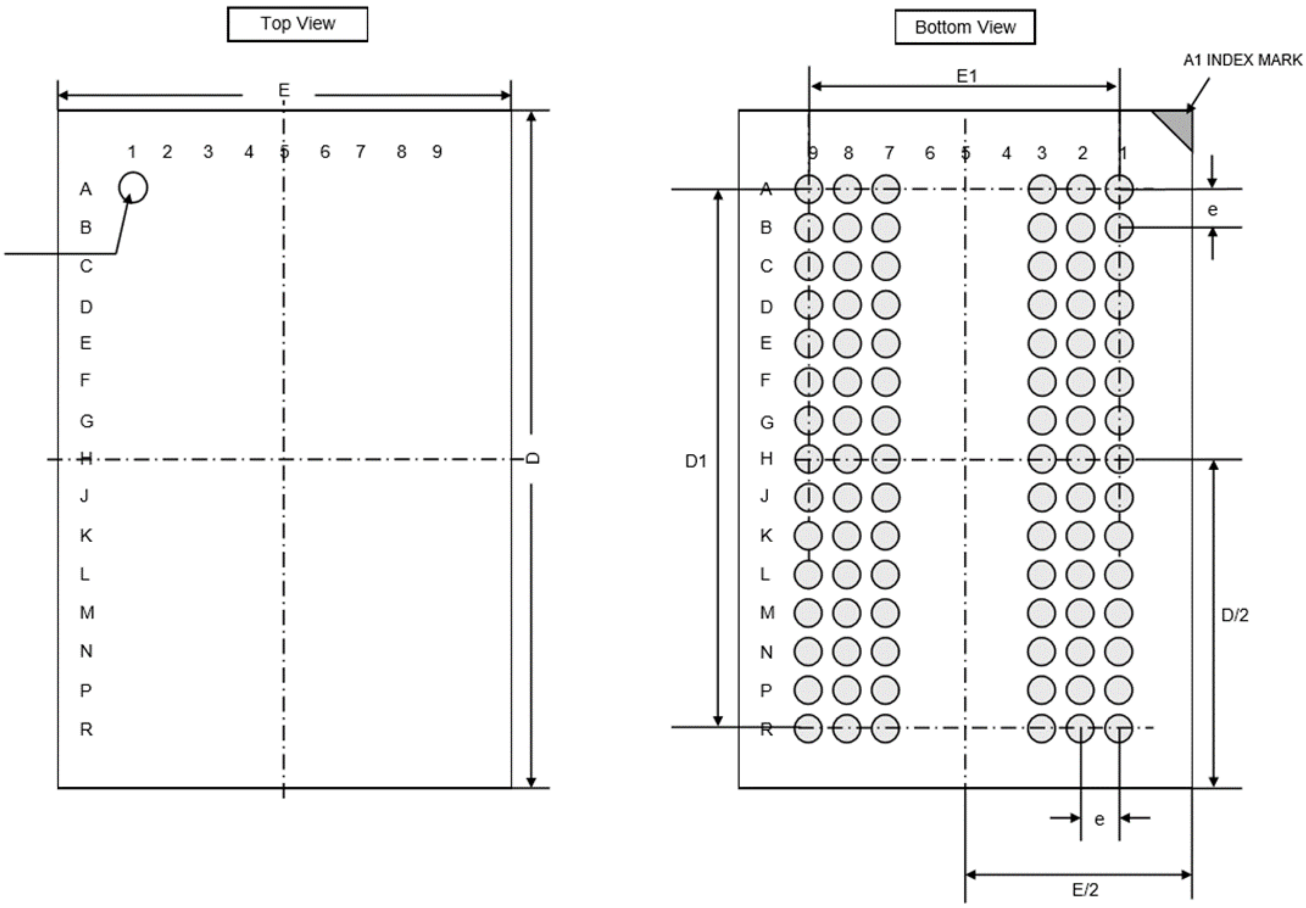
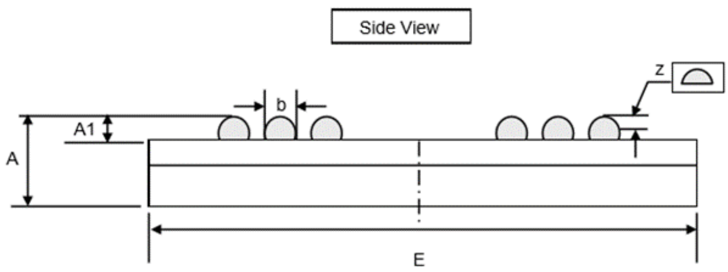
Figure 42. 90 BALL FBGA

Unit: millimeters





Unit : mm

-	Min	Typ	Max
A	-	-	1.00
A1	0.25	0.30	0.35
E	-	8.00	-
E1	-	6.40	-
D	-	13.00	-
D1	-	11.20	-
e	-	0.80	-
b	0.35	0.40	0.45
z	-	-	0.10

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